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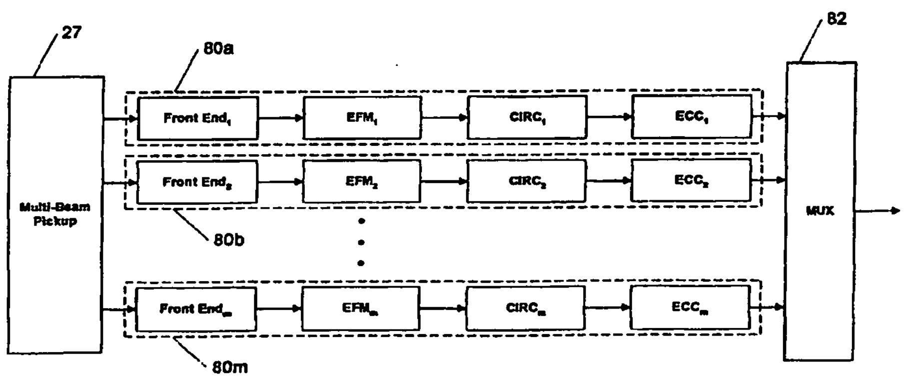

(57) Abstract

Methods and apparatus are provided for synchronously reading data from multiple tracks of an optical disk using multiple illumination beams. Circuitry is provided for use with a photodetector array to read and buffer data in parallel from the multiple adjacent tracks, while asynchronously providing processed data to a host processor. Circuitry is further provided for concurrently processing the signals read from the multiple data tracks to recover the data stored in the tracks.

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METHODS AND APPARATUS FOR CONCURRENTLY PROCESSING DATA FROM MULTIPLE TRACKS OF AN OPTICAL STORAGE MEDIUM

Field of the Invention

This invention relates to methods and apparatus for retrieving information from an optical disk at high data rates by simultaneously and synchronously reading multiple adjacent tracks.

Background of the Invention

Due to their high storage density, long data retention life, and relatively low cost, optical disks are becoming increasingly popular as a means to distribute information. Large format disks have been developed for storing full length motion pictures. The compact disk (CD) format was developed and marketed for the distribution of musical recordings and has replaced vinyl records. High-capacity, read-only data storage media, such as CD-ROM and DVD, have become prevalent in the personal computer field, to the point that the DVD format may soon replace videotape as the distribution medium for video information.

An optical disk is made of a transparent disk or substrate in which data, in the form of a serial bit-stream, are encoded as a series of pits in a

reflective surface within the disk. The pits are arranged along a spiral or circular track. Data are read from the optical disk by focusing a low power laser beam onto a track on the disk and detecting the light reflected from the surface of the disk. By rotating the optical disk, the light reflected from the surface of the disk is modulated by the pattern of the pits rotating into and out of the laser's field of illumination. Optical and imaging systems detect the modulated, reflected, laser light and produce an electrical signal which may be decoded to recover the digital data stored on the optical disk. The recovered digital data, which may include error correcting codes and additional subcoded information, are further processed to recover the stored data which may then be converted to audio signals, or used as executable programs and data depending on the type of optical disk being read.

To be able to retrieve data from anywhere on an optical disk, the optical systems include a pickup assembly which may be positioned to read data from any disk track. Servo mechanisms are provided for focusing the optical system and for keeping the pickup assembly positioned over the track, despite disk warpage or eccentricity.

Because in most previously known systems the data are retrieved from the disk serially, i.e. one bit at a time, the maximum data transfer rate for an optical disk reader is determined by the rate at which the pits pass by the pickup assembly. The linear density of the bits and the track pitch are fixed by the specification of the particular optical disk format. For example, CD disks employ a track pitch of

1.6 µm, while DVD employs a track pitch only about one-half as wide.

Previously known methods of increasing the data transfer rate of optical disk readers have focused on increasing the rate at which the pits pass by the pickup assembly by increasing the rotational speed of the disk itself. Currently, drives with rotational speeds of up to 16× standard speed are commercially available, and even faster speeds have been achieved by moving to constant angular velocity designs. However higher disk rotational speeds place increasing demands on the optical and mechanical subsystems within the optical disk player, create greater vibration, and may make such players more difficult and expensive to design and manufacture.

Other previously known techniques for increasing average data transfer rates involve methods to intelligently anticipate future read requests by a host processor. It has been observed that data access by computers frequently exhibit "locality of reference," which means that a future data access will be local, in either space or time, to a previous data access. Thus a CD-ROM drive or controller can "read ahead" and buffer the data that the host processor is likely to request next. When the host processor next requests data from the optical disk drive, the drive first checks if the requested data have already been read and buffered. If the data have already been buffered, the drive simply sends the buffered data to the host, avoiding the delays associated with repositioning the pickup assembly and reading data from the optical disk itself. While such caching techniques may speed up average data access times, the maximum data transfer rate is still limited by the rotational

velocity of the optical disk within the optical disk reader.

Commonly assigned U.S. patent 5,627,805 describes a system to increase disk reading speeds by reading multiple tracks simultaneously. The data is read using a wide area reading beam, which is focussed onto a plurality of tracks on the disk. A detector comprising a matrix of photo-detector elements provides an image of the wide area, from which track signal data for each of a plurality of tracks is extracted by a virtual tracking system. Alternatively, the track data signals may be provided by an optical pickup which uses multiple beams to simultaneously read multiple tracks of an optical disk. The track data signals are then sampled, to produce a plurality of digital data streams, which are multiplexed into a single data stream before demodulation, decoding, and error correction.

Since the multiplexed data stream contains data from multiple tracks, which may be read from a disk that is spinning at multiple times the standard speed, the rate at which data in the multiplexed stream must be processed may be very high. For example, in a multi-beam CD-ROM reader that reads seven tracks simultaneously and spins the disk at 8× the standard speed (giving the approximate equivalent of a 56× drive), the data rate in the multiplexed data stream will be approximately 240 million bits per second in the demodulation stage (17 million words per second at 14 bits per word). By the time the data reaches the error correction stage, the required data rate will have dropped to approximately 79 million bits per second (9.9 million bytes per second). As can be seen, the rate at which data in such a system must be

processed requires use of high performance devices to perform the functions at each of the stages in the processing chain.

The present application is directed to an improvement in the system described in the above-incorporated patent, wherein the multiplexer is moved to a later position in the processing chain, so that the plurality of data streams from multiple tracks on the disk may be demodulated, decoded, and error corrected before being multiplexed into a single data stream. Apparatus in accordance with the present invention may use a plurality of inexpensive, relatively low performance devices to perform the steps of demodulation, decoding, and error correction, while delivering throughput similar to that achieved by a high performance device performing these operations on a single multiplexed stream of data. Using the techniques of the present invention, it may be possible to construct a high performance system for processing the multiple data streams read from an optical disk, and which has a higher throughput than other similar systems, using standard low cost components.

It would therefore be desirable to provide apparatus and methods which permit simultaneous processing of data from multiple tracks in an optical disk reader.

It would also be desirable to provide demodulation, decoding, and error correction circuitry having higher throughput and at lower cost than previously known circuitry for processing the data from multiple tracks in an optical disk reader.

Summary of the Invention

In view of the foregoing, it is an object of the present invention to provide apparatus and methods for simultaneous processing of data from multiple tracks in an optical disk reader.

It is a further object of this invention to provide demodulation, decoding, and error correction circuitry having higher throughput and faster time to market than previously known circuitry for processing the data from multiple tracks in an optical disk reader.

These and other objectives of the invention are accomplished by placing the multiplexer in a position late in the processing stream, so that the data from the multiple tracks remain separate through the processing stages of demodulation, decoding, and error correction. Implementation of this scheme requires providing multiple demodulation, decoding, and error correction units.

Alternatively, the multiplexer may be placed in the processing chain between the demodulation stage and the decoding stage, so that demodulation is performed in parallel on the multiple data streams, but decoding and error correction are performed on a single, multiplexed data stream. The multiplexer could also be placed in the processing stream between the decoding stage and the error correction stage, so that demodulation and decoding are performed in parallel on the multiple data streams, and error correction is performed on a single, multiplexed data stream.

Further features of the invention, its nature and various advantages will be more apparent from the accompanying drawings and the following detailed description of the preferred embodiments.

Brief Description of the Drawings

FIG. 1 is an illustrative block diagram of a previously known single beam optical disk reader;

FIG. 2 is an illustrative block diagram of a multi-beam optical disk reader;

FIG. 3 is a block diagram of a multi-beam optical disk reader built in accordance with the principles of the present invention;

FIG. 4 is a block diagram of the front end circuitry for extracting data from the signals output by the pickup assembly of FIG. 3;

FIGS. 5A, B, and C are block diagrams of the demodulator circuitry, decoder circuitry, and error correction circuitry, respectively, of the optical disk reader of FIG. 3;

FIGS. 6 and 7 are block diagrams of alternative embodiments of multi-beam optical disk readers built in accordance with the principles of the present invention; and

FIG. 8 is a block diagram of an alternate arrangement for the processing chain of an optical disk reader built in accordance with the principles of the present invention.

Detailed Description of the Invention

By way of overview, a brief description of the components and operation of a previously known optical disk reader 10 is provided with respect to FIG. 1. The detailed description of the design and operation of such previously known optical disk readers may be found, for example, in Compact Disk Technology, H. Nakajima and H. Ogawa, published by Ohmsha, Ltd., Japan (1992), translated by Aschmann, C., IOS Press, Inc., Burke, Virginia, and The Compact Disk Handbook, Ken C. Pohlmann (2nd Ed. 1992), A-R Editions, Inc., Madison, Wisconsin, both of which are incorporated herein in their entirety by this reference. An overview of multi-beam optical disk reader 25 is given with respect to FIG. 2.

It will of course be understood that the systems of FIGS. 1 and 2 are merely illustrative of the various types of optical disk apparatus in which the methods and apparatus of the present invention may be employed. Applicants expect that the invention described herein may be advantageously employed in any multi-beam optical disk system, including DVD systems.

Overview Of A Prior Art Optical Disk System

Referring to FIG. 1, illustrative previously known optical disk reader 10 comprises a spindle motor 11 that rotates optical disk 100 at high speed and pickup 12 including an illumination source and a photodetector for generating electrical signals representative of information-bearing pits formed in a reflective surface within optical disk 100. The electrical signals from the photodetector of pickup 12 are then passed to front end circuitry 13 for extracting a digital data signal. Under the control of

controller 24, the data signal is further processed by eight-to-fourteen (EFM) demodulation circuitry 17, Cross Interleaved Reed-Solomon Code (CIRC) decoding circuitry 18, error correction code (ECC) circuitry 19, and subcode circuitry 16. Controller 24 also controls focus and tracking circuitry 14, as well as buffer 20 and interface 22.

For a digital audio system, the data signals may be processed into suitable analog signals (using circuitry not shown) connected to audio means 21. Similarly, if the optical disk contains video images, the data signals may be processed for display on a TV or monitor. In computer applications the data signals are typically transferred from buffer 20 to host processor 23 via interface 22.

Spindle motor 11 spins optical disk 100 at a speed that depends upon the radial location of pickup assembly 12 (for example, for a 1× CD-ROM spindle speed, approximately 200-500 RPM), to maintain a constant linear velocity of an optical disk track relative to pickup assembly 12. For a CD-ROM format, this linear velocity is generally 1.4 m/s, while for the DVD format it approaches 4 m/s. Pickup assembly 12 typically includes a laser diode that illuminates only a single data track on optical disk 100 and an optical sensor onto which an image reflected from the optical disk is projected. The intensity, or other property, of the light beam reflected from the surface of optical disk 100 is modulated by inhomogeneities in the reflective surface of the optical disk (i.e., bumps or pits, referred to hereinafter as "data spots") arranged in spiral or circular tracks on optical disk 100.

Pickup assembly 12 includes circuitry to generate an electronic signal representative of the

modulation in the illumination impinging upon its optical sensor due to the presence of the data spots. To ensure that the laser illumination remains focused on the reflective surface of optical disk 100, pickup assembly 12 also provides signals to focus and tracking subsystem 14.

The data spots are recorded on optical disk 100 using a modulation code that permits a data clock to be recovered from the data as it is read off of the optical disk. Clock circuitry 15 includes phase-locked-loop (PLL) circuitry for recovering the data clock from, and maintaining the data clock in synchrony with, the modulated electronic signal from pickup assembly 12. In addition to being used for extracting the data from the modulated signal, the data clock is representative of the linear velocity of the data track relative to pickup assembly 12 and may be used as a feedback signal to control the speed of spindle motor 11 to maintain a constant linear velocity.

Front end circuitry 13 uses the data clock from PLL 15 to recover a serial stream of bits from the electronic signal. Front end circuitry 13 contains additional circuitry to identify synchronization codes in the bit stream so that the serial bit stream may be correctly assembled into multi-bit data words which are transferred to demodulation circuitry 17. Demodulation circuitry 17 may be programmed for eight-to-fourteen demodulation, eight-to-fifteen demodulation (as in the SD systems), eight-to sixteen demodulation (EFM Plus), or may use another suitable demodulation scheme. The demodulated data words, or symbols, are then assembled into blocks and decoded by CIRC decoder 18 using a form of Cross Interleaved Reed-Solomon code, for example, CIRC for CD-formats and PI PO structure for DVD.

Demodulated data words are also provided to subcode processor 16 which extracts data, such as block numbers, or song titles, that may be recorded in the subcode channels embedded in each block of data words.

For video and audio optical disk players, the data from CIRC decoder 18 represents, in digital form, the video or audio signal that was originally recorded and stored on the disk. These signals may then be converted to analog signals and the original recorded signal reproduced using conventional audio or video devices 21. Errors in the recovered audio or video signals are handled by interpolation and filtering circuitry (not shown) to calculate a value to use in place of the erroneous data. Because of the interpolation process, isolated errors in an audio or video signal are unlikely to be noticed when listening to the audio or viewing the video signals.

However, since a single bit error in data representing a computer program may render the program inoperable or the data unusable, optical disks used for the storage and distribution of data and programs must have very low data error rates. To reduce the data error rates to acceptably low levels, error correction codes (ECC) are added to the data when it is recorded to the disk. ECC circuitry 19 uses error correcting codes to detect and possibly correct errors in the data. Finally, the data are buffered in memory buffer 20 for transfer to host processor 23 via interface circuitry 22. Controller 24 coordinates operation of each of the optical disk reader subsystems and to control the operation of the optical disk reader as a whole.

Referring now to FIG. 2, an optical disk reader similar to that described in U.S. Patent Number

5,627,508 is described. Apparatus 25 provides a high data transfer rate by reading multiple tracks of data from an optical disk simultaneously. Much of the circuitry of FIG. 2 may be common to or readily adapted from the circuitry of the system of FIG. 1. Accordingly, the following description focuses on the differences between previously known single beam optical disk reader 10 of FIG. 1, and multi-beam optical disk reader 25.

In particular, apparatus 25 includes a multi-beam, multi-detector pickup assembly 27 that simultaneously illuminates and reads multiple adjacent data tracks of disk 100; phase-lock loop circuitry that permits a clock 29 associated with a reference track to be used for synchronizing the recovery of data from neighboring tracks; and a parallel write/asynchronous read architecture that enables blocks of data to be read from the optical disk, processed and written to a buffer in parallel while being asynchronously retrieved from the buffer by a host computer.

Multi-beam optical disk reader 25 of FIG. 2 includes pickup assembly 27 including a source of laser illumination, a diffraction grating for splitting the laser illumination into three or more illumination beams and a corresponding number of photodetectors onto which multiple illumination beams, reflected from the optical disk, are focused by an optical system. Each of the multiple photodetectors in pickup assembly 27 generates an electrical signal representing data read from a corresponding data track on optical disk 100, and provides that electrical signal to front end circuitry 30.

Front end circuitry 30 of FIG. 2 performs a function similar to that of front end circuitry 13 of

FIG. 1, except that multiple bit streams are processed concurrently, so additional circuitry is provided for buffering and synchronizing data transfers to subsequent processing circuitry. Front end circuitry 30 also includes a multiplexer for routing multiple data streams to demodulation circuitry 32 in the form of a single multiplexed data stream.

Demodulation circuitry 32, subcode circuitry 31, decoder circuitry 34, and error correction circuitry 36 of optical disk reader 25 are all similar in operation to their counterparts in optical disk reader 10 of FIG. 1. They differ principally in that they may be required to handle a much greater data throughput than similar circuitry used in single-beam optical disk reader 10.

Buffer memory 33 is provided to buffer the data read from the multiple data tracks, and to decouple the process of reading data from optical disk 100 from the process of transferring the data to host processor 37. Buffer 33 therefor is large enough to hold about as many data blocks from multiple data tracks of optical disk 100 as can be read in one revolution of optical disk 100. Controller 38 maps data from the multiple data tracks to memory 33 so that individual data blocks will be correctly assembled without overwriting one another. As will be appreciated by those of skill in the art of buffer design, this mapping may be either dynamic or static.

Description of the Present Invention

Referring to FIG. 3, multi-beam optical disk reader 40, constructed in accordance with the principles of the present invention is described. Multi-beam optical disk reader 40 is very similar to

multi-beam optical disk reader 25, of FIG. 2, except that multiple data streams are processed concurrently through the entire processing chain, rather than just the front end. Instead of using a multiplexer in front end circuitry 42 to combine the multiple data streams into a single multiplexed data stream, multi-beam optical disk reader 40 places multiplexer 52 at the end of the processing chain, after the data are read, demodulated, decoded, and error corrected.

Front end circuitry 42 recovers multiple streams of bits from the electronic signals corresponding to the multiple tracks read by multi-beam optical pickup 27, by recovering the clock for one track, and adjusting that clock signal to account for differences in the linear velocities of the tracks. Alternatively, front end circuitry 42 may use a separate phase-locked loop (PLL) for each track to regenerate a clock signal for each of the tracks being read. Front end circuitry 42 also assembles the streams of bits into multi-bit data words which are transferred to demodulation circuitry 44 as multiple streams of data words.

Demodulation circuitry 44 demodulates each of the streams of data words into demodulated data words, or symbols. These symbols are assembled into frames, each containing multiple symbols, which are made available to decoder circuitry 46 as multiple streams of frames. Demodulation circuitry 44 may be programmed for eight-to-fourteen demodulation, eight-to-fifteen demodulation (as in the SD systems), eight-to sixteen demodulation (EFM Plus), or may use another suitable demodulation scheme. Demodulated data words are also provided in multiple streams to subcode processor 43 which extracts data, such as frame numbers, or song

titles, that may be recorded in the subcode channels embedded in each frame of data words.

Decoder circuitry 46 uses a form of Cross Interleaved Reed-Solomon Code, such as CIRC for CD-formats and PI PO structure for DVD, to decode the frames of data received in each of the data streams. The decoded frames are then assembled into sectors, which contain the data from multiple frames, and are made available to error correction circuitry 48 as multiple streams of sectors. Each sector contains a sector type identifier, used for determining which type of error correction or other processing to perform on the sector. Sectors also contain synchronization codes, data, and may contain error correction codes.

If the sector type identifier indicates that a sector contains error correction codes, error correction circuitry (ECC) 48 uses the error correction codes to detect and possibly correct errors in the data. The corrected data from each of the data streams is then made available to buffer memory 50 through multiplexer (MUX) 52. Buffer memory 50 uses MUX 52 to select one of the data streams, and transfers one sector of corrected data from ECC circuitry 48 to memory. Buffer memory 50 permits stored data to be transferred to host processor 23 via interface circuitry 22.

Controller 54 coordinates operation of each of the optical disk reader subsystems and controls the operation of the optical disk reader as a whole.

FIG. 4 shows a detailed view of front end circuitry 42, constructed using a separate PLL for each track. Multi-beam pickup assembly 27 outputs track data signals, $T_1 \ldots T_m$, corresponding to m tracks being

read. Since an accurate data clock is needed to extract data from a track data signal, and the signals from each track will differ in frequency and phase, the track data signals $\mathbf{T}_1 \ldots \mathbf{T}_m$ are provided to separate phase-locked loops (PLLs) 56 which are used to recover a clock signal for each track. These clock signals are used by data samplers 57 to recover digital data from the tracks. The serial bit streams are assembled into parallel data words and are then sent to first-in/first-out buffers (FIFOs).

For an 8× multi-beam CD-ROM reader, each stream in front-end circuitry 42 will produce approximately 2.5 million 14-bit data words per second, which can easily be handled by inexpensive commercially available circuitry. By contrast, if the data from an 8× speed, seven-beam system were combined into a single data stream at the front end stage of processing, the data rate would be approximately 17.5 million 14 bit words per second.

It will, of course, be understood that methods and apparatus which permit a common clock to be used to recover clocks for all of the track data signals, alternatively could be used in the front end circuitry of a multi-beam optical disk reader built in accordance with the principles of the present invention.

Referring now to FIGS. 5A-C, demodulator circuitry 44, decoder circuitry 46, and error correction circuitry 48 are shown. Demodulator circuitry 44, shown in FIG. 5A, comprises *m* single-stream demodulator units 60, each of which handles the data words sent to it through one FIFO 58 of front end circuitry 42. Each of demodulator units 60 demodulates

data words from one track into demodulated data words, or symbols, and assembles the symbols into frames. Additionally, demodulator units 60 may extract subcode data from the data stream, and send the subcode data to subcode processor 43.

For an 8× multi-beam CD-ROM reader, each demodulator unit 60 assembles 58,800 frames per second, each frame containing 32 bytes, for a total of approximately 1.9 million bytes per second. If the data from a seven beam, 8× system were combined into a single stream at the demodulator stage, the combined data stream would have a data rate of approximately 13.2 million bytes per second. Thus, applicant expects that retaining multiple data streams will permit use of a greater number of lower cost (slower) components.

FIG. 5B shows decoder circuitry 46, which comprises one single-track Cross Interleaved Reed-Solomon Code (CIRC) decoder unit 62 for each of the *m* data tracks being processed. Data from demodulator units 60 are sent into CIRC decoder units 62. Each of CIRC decoder units 62 decodes data from a single track, and assembles the data into sectors, which are sent to error correction circuitry 48.

For an 8× multi-beam CD-ROM reader, each CIRC decoder unit 62 assembles 600 sectors per second, each sector containing 2352 bytes, for a total of approximately 1.4 million bytes per second. If the data from a seven beam, 8× system were combined into a single stream at the decoder stage, the combined data stream would have a data rate of approximately 9.9 million bytes per second.

FIG. 5C shows error correction circuitry 48, which comprises one single-track error correction unit

64 for each of the *m* data tracks being processed. Data from CIRC decoder units 62 are sent into the error correction units 64. Each of the error correction units 64 examines a sector-type identifier byte for each sector sent by CIRC decoder units 62 to determine which error correction technique (if any) to perform on a sector. If error correction is required, error correction unit 64 applies the error correction technique indicated by the sector-type identifier byte, and outputs the corrected sector data. If the sector is of a type which does not require correction, error correction unit 64 need only strip any synchronization bytes, or other extraneous formatting from the sector data.

For an 8× multi-beam CD-ROM reader, each error correction unit 64 processes 600 sectors per second, each sector containing up to 2336 bytes of data, plus four bytes of header information, for a total of approximately 1.4 million bytes per second. A multiplexer combining data from a seven beam, 8× system after the error correction stage would need to be able to handle a throughput of approximately 9.8 million bytes per second.

Referring now to FIG. 6, an alternate embodiment of a multi-beam optical disk reader built in accordance with the principles of the present invention is shown. As will be understood from the above discussion, the data rate of a single multiplexed data stream becomes smaller in later stages of the processing chain. It may therefore be practical to use circuitry which processes the track data concurrently for the early stages in the processing chain, such as the front end processing and demodulation, where the

data rate is highest, while using circuitry which processes a single data stream for later stages, such as decoding and error correction. Accordingly, in optical disk reader 60, Multiplexer 62 has been placed between demodulation circuitry 44 and decoder circuitry 34 in the processing chain. Multiplexer 62 combines the data from all of the single-track demodulation units of demodulation stage 44 into a single data stream. As shown in FIG. 6, multiplexer 62 sends the combined stream of data to buffer memory 50, where it is stored until the frames are requested by host 23, or are no longer needed. Alternatively, if later stages are capable of handling the throughput required to process the combined data stream, buffer memory 50 can be placed at the end of the processing chain, and the combined data stream from multiplexer 62 may be sent directly into decoder stage 34.

FIG. 7 shows another alternative embodiment, in which multiplexer 66 is located between decoder circuitry 46 and error correction circuitry 36 in the processing chain. Multiplexer 66 combines the data streams from the single-track decoder units in decoder stage 46 into a single data stream, which is stored in buffer memory 50. If the error correction stage is capable of handling the throughput required to process the combined data stream, buffer memory 50 may be placed at the end of the processing chain, after error correction stage 36.

FIG. 8 shows a yet further alternative arrangement of the processing chain for a multi-beam optical disk reader constructed in accordance with the principles of the present invention. The processing chain shown in FIG. 8 is arranged according to which beam is being processed, rather than according to

function. Thus, data from the first beam are sampled, demodulated, decoded, and error corrected by data stream processor 80a, while data from the second beam are processed by data stream processor 80b, and so on. Multiplexer (MUX) 82 multiplexes data from the data streams into a single data stream. Embodiments in which multiplexer 82 is located after the demodulator (EFM) stage or the decoder (CIRC) stage may also be arranged according to the beam being processed, rather than by function.

Arranging the circuitry as shown in FIG. 8 permits standard, relatively inexpensive parts, which were designed for use in single-beam optical disk readers to be used to build a multi-beam optical disk reader in accordance with the principles of the present invention. Commercially available CD controllers combine several of the processing stages of a single-beam optical disk reader into a single integrated circuit. The OTI-975, by Oak Technology of Sunnyvale, California, for example, is capable of performing decoding and error correction on a single data stream for a 16× CD-ROM reader. Other commercial parts manufactured by Philips Electronics N.V., and Sony Semiconductor provide similar functions, and perform clock recovery (using PLLs), data sampling, and demodulation for use with a single-beam optical disk reader. Data stream processors 80a-80m could be assembled from such standard parts, and then combined using MUX 82 to form the processing chain for a multi-beam optical disk reader in accordance with the arrangement of the circuitry shown in FIG. 8.

While preferred illustrative embodiments of the present invention are described above, it will be evident to one skilled in the art that various changes

and modifications may be made without departing from the invention. It is intended in the appended claims to cover all such changes and modifications which fall within the true spirit and scope of the invention.

What Is Claimed Is:

1. Apparatus for simultaneously reading multiple data tracks of an optical disk, the apparatus comprising:

a pickup assembly providing a plurality of data signals corresponding to data stored in a plurality of data tracks of an optical disk;

sampling circuitry for recovering a plurality of digital data streams from the plurality of data signals;

a multiplexer for combining the plurality of digital data streams into a single data stream; and

processing circuitry for extracting formatted data from the plurality of digital data streams, the processing circuitry comprising a concurrent portion, disposed before the multiplexer, wherein the plurality of digital data streams are processed simultaneously, and a serial portion, disposed after the multiplexer, wherein the single data stream is processed to produce the formatted data.

2. The apparatus as defined in claim 1, wherein the processing circuitry comprises a plurality of processing stages which are applied to the plurality of digital data streams to extract the formatted data.

3. The apparatus as defined in claim 2, wherein the processing stages include a demodulation stage, a decoding stage, and an error correction stage.

4. The apparatus as defined in claim 3, wherein the processing circuitry includes a buffer, in which data may be temporarily stored.

5. The apparatus as defined in claim 4, wherein the demodulation stage, decoding stage, and error correction stage are all part of the concurrent portion of the processing circuitry, the buffer is part of the serial portion of the processing circuitry, and the multiplexer is disposed between the error processing stage and the buffer.

6. The apparatus as defined in claim 4, wherein the demodulation stage is part of the concurrent portion of the processing circuitry, and the decoding stage, error correction stage, and buffer are part of the serial portion of the processing circuitry.

7. The apparatus as defined in claim 6, wherein the multiplexer is interposed between the demodulation stage, and the buffer.

8. The apparatus as defined in claim 6, wherein the multiplexer is interposed between the demodulation stage and the decoding stage.

9. The apparatus as defined in claim 4, wherein the demodulation stage and decoding stage are part of the concurrent portion of the processing circuitry, and the error correction stage and buffer are part of the serial portion of the processing circuitry.

10. The apparatus as defined in claim 9, wherein the multiplexer is interposed between the decoding stage and the buffer.

11. The apparatus as defined in claim 9, wherein the multiplexer is interposed between the decoding stage and the error correction stage.

12. The apparatus as defined in claim 1, wherein the sampling circuitry comprises a clock recovery circuit for each of the data signals.

13. The apparatus as defined in claim 12, wherein each clock recovery circuit comprises phase-locked loop circuitry.

14. The apparatus as defined in claim 1, wherein the sampling circuitry comprises synchronizing circuitry for permitting a single clock recovery circuit to be used to sample the plurality of data signals, the synchronizing circuitry correcting for variations in the linear velocities of the plurality of data tracks.

15. The apparatus as defined in claim 3, wherein the demodulation stage comprises circuitry implementing any one of eight-to-fourteen demodulation, eight-to-fifteen demodulation, or eight-to sixteen demodulation.

16. The apparatus as defined in claim 3, wherein the decoding stage comprises circuitry implementing a cross-interleaved Reed-Solomon decoder.

17. A method for processing a plurality of data signals simultaneously read from a plurality of data tracks of an optical disk to extract formatted data, the method comprising the steps of:

sampling the plurality of data signals to produce a plurality of digital data streams;

concurrently processing the plurality of digital data streams;

multiplexing the plurality of digital data streams into a single serial data stream; and

processing the serial data stream to produce the formatted data.

18. The method of claim 17, wherein the step of concurrently processing the plurality of digital data streams further comprises the steps of:

concurrently demodulating the plurality of digital data streams;

concurrently decoding the plurality of digital data streams; and

concurrently error correcting the plurality of digital data streams.

19. The method of claim 18, wherein the step of multiplexing the plurality of digital data streams follows the step of concurrently error correcting the plurality of digital data streams.

20. The method of claim 17, wherein the step of concurrently processing the plurality of digital data streams further comprises the step of concurrently demodulating the plurality of digital data streams, and the step of processing the serial data stream further comprises the steps of:

decoding the serial data stream; and

error correcting the serial data stream.

21. The method of claim 20, wherein the step of multiplexing the plurality of digital data streams follows the step of concurrently demodulating the plurality of digital data streams.

22. The method of claim 17, wherein the step of concurrently processing the plurality of digital data streams further comprises the steps of:

concurrently demodulating the plurality of digital data streams; and

concurrently decoding the plurality of digital data streams; and

the step of processing the serial data stream further comprises the step of error correcting the serial data stream.

23. The method of claim 22, wherein the step of multiplexing the plurality of digital data streams follows the step of concurrently decoding the plurality of digital data streams.

24. The method of claim 17, wherein the step of sampling the plurality of data signals further comprises the step of generating a separate clock signal for each one of the plurality of data signals.

25. The method of claim 17, wherein the step of sampling the plurality of data signals further comprises the step of correcting a single clock signal to account for differences in plurality of data signals caused by variations in the linear velocity of the plurality of data tracks.

26. Apparatus for concurrently processing a plurality of streams of data simultaneously read from a plurality of tracks of an optical disk, the apparatus comprising:

a plurality of data stream processing circuits, each data stream processing circuit processing one of the plurality of data streams; and

a multiplexer for combining the outputs of the plurality of data stream processing circuits into a single data stream.

27. Apparatus as defined in claim 26, wherein each one of the plurality of data stream processing circuits comprises circuitry for demodulating a data stream.

28. Apparatus as defined in claim 27, wherein each one of the plurality of data stream processing circuits comprises circuitry for decoding a data stream.

29. Apparatus as defined in claim 28, wherein each one of the plurality of data stream processing circuits comprises circuitry for error correcting a data stream.

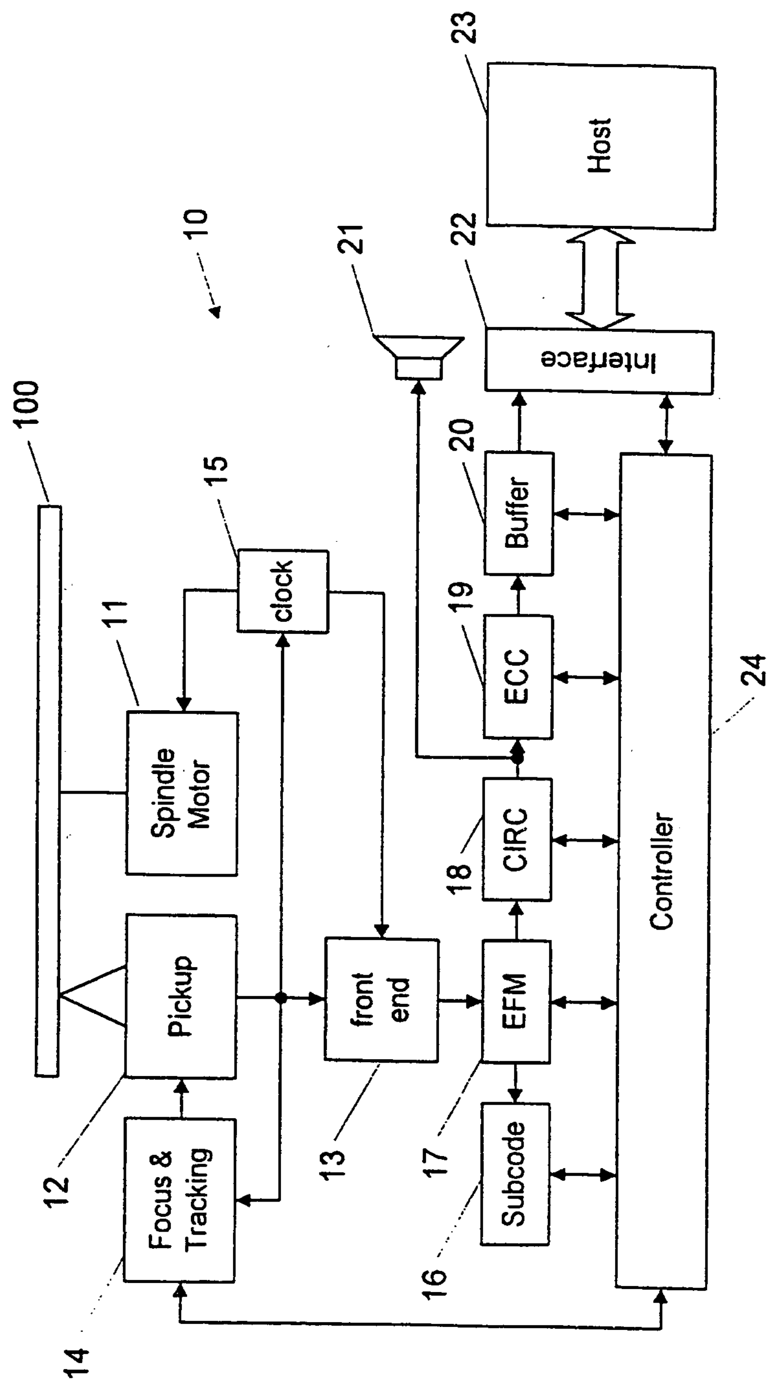

FIG. 1 (Prior Art)

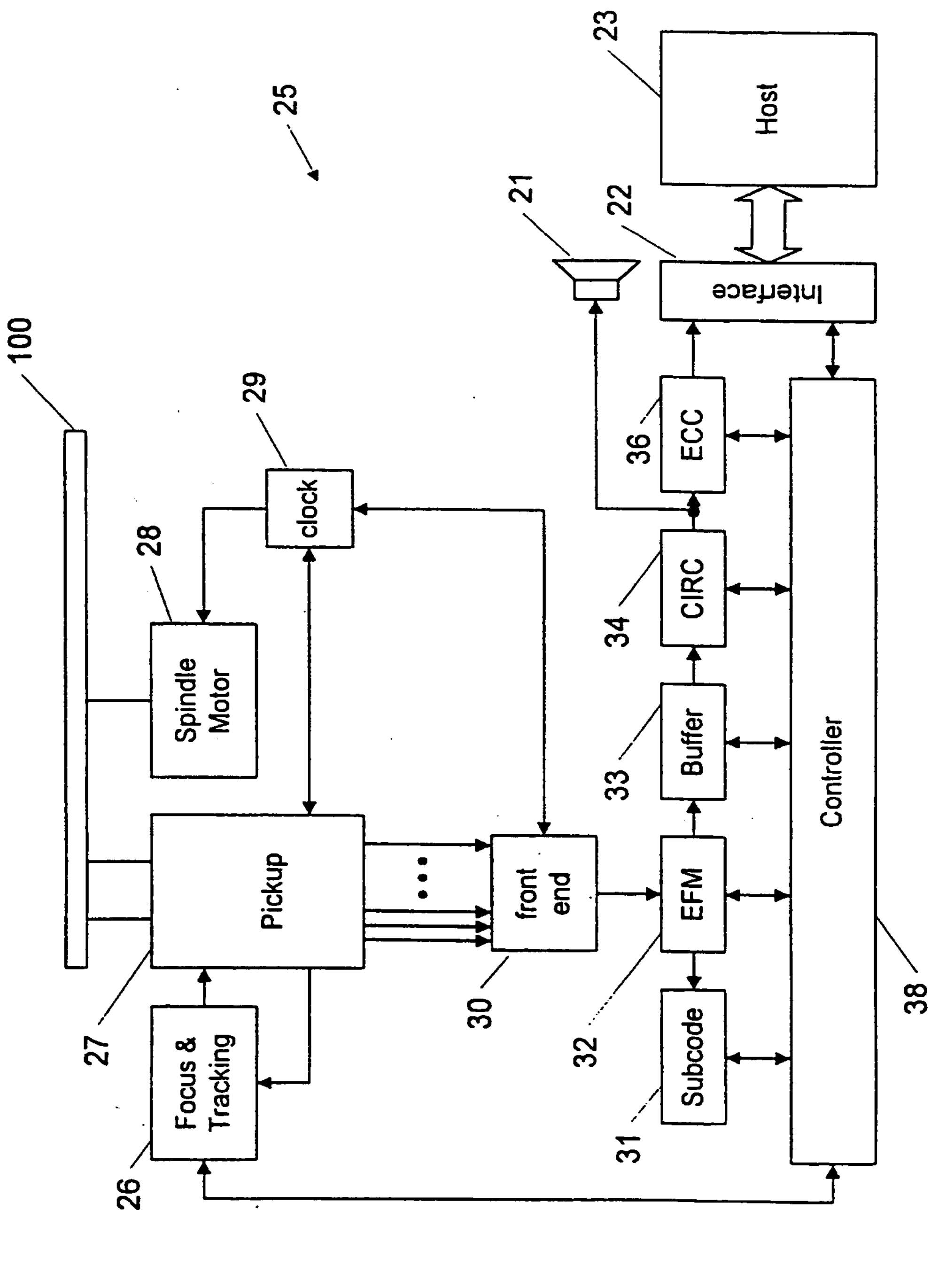
100
25
29
clock
28
Spindle Motor
Pickup
27
Focus & Tracking
26
front end
30
EFM
32
Subcode
31
Buffer
33
CIRC
34
ECC
36
21
22
Interface
23
Host
Controller
38

FIG. 2

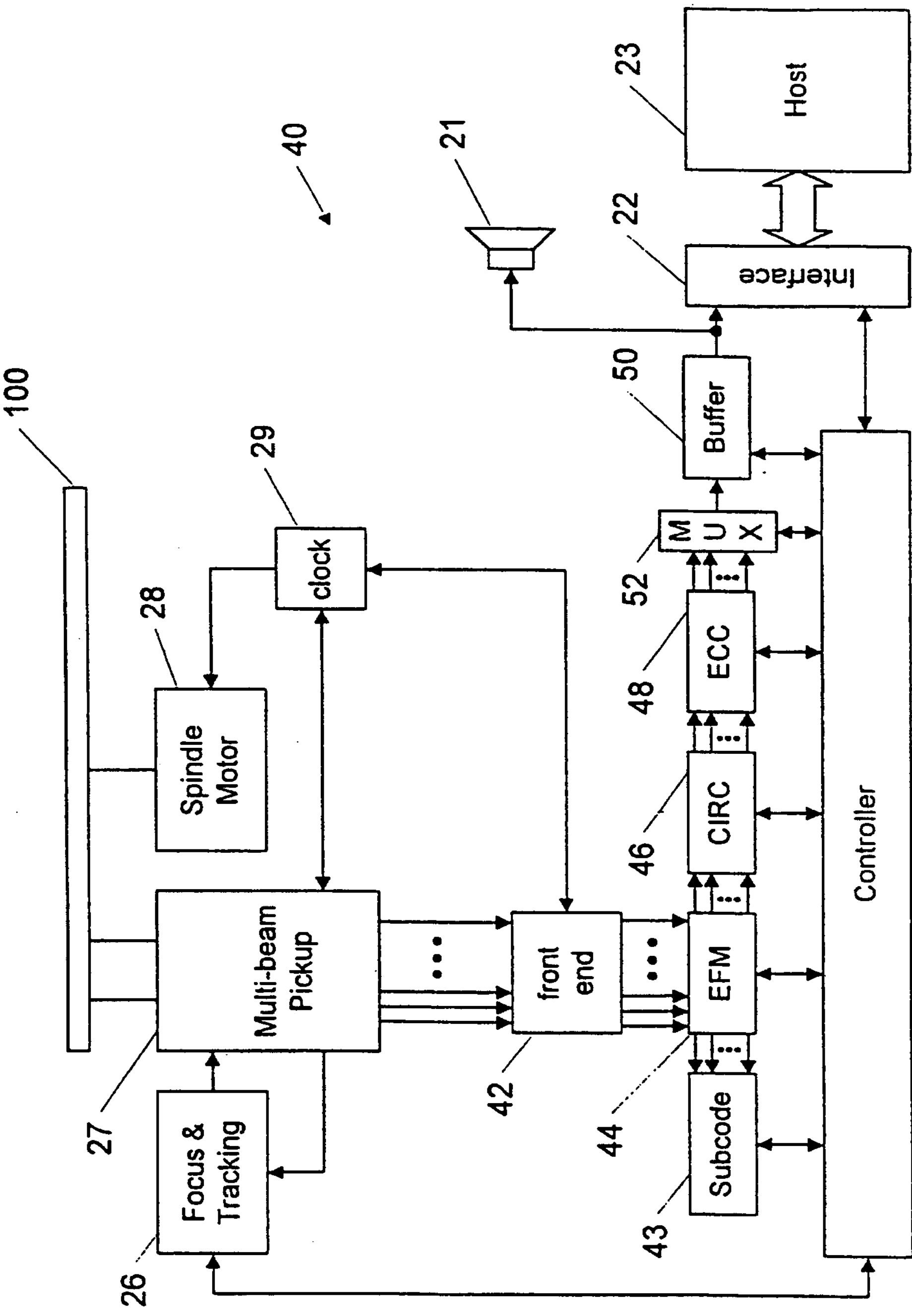
100
40
21
23
Host
22
Interface
29
clock
28
Spindle Motor
50
Buffer
52
MUX
48
ECC
46
CIRC
Multi-beam Pickup
front end
EFM
Subcode
Controller
Focus & Tracking
27
42
44
43
54
26

FIG. 3

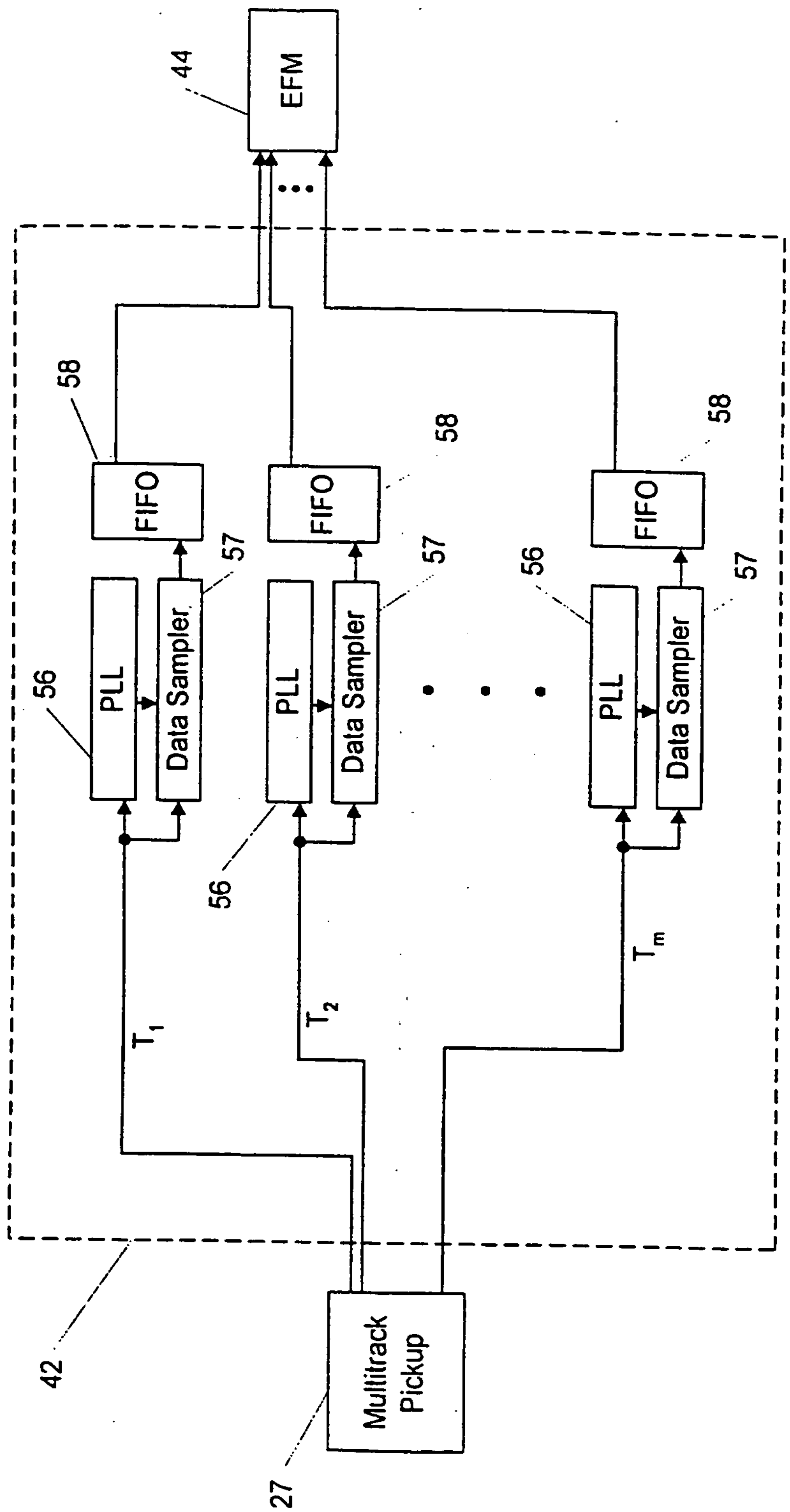
EFM
44
58
FIFO
57
Data Sampler
PLL
56
T_1
T_2
T_m
42
Multitrack Pickup
27

FIG. 4

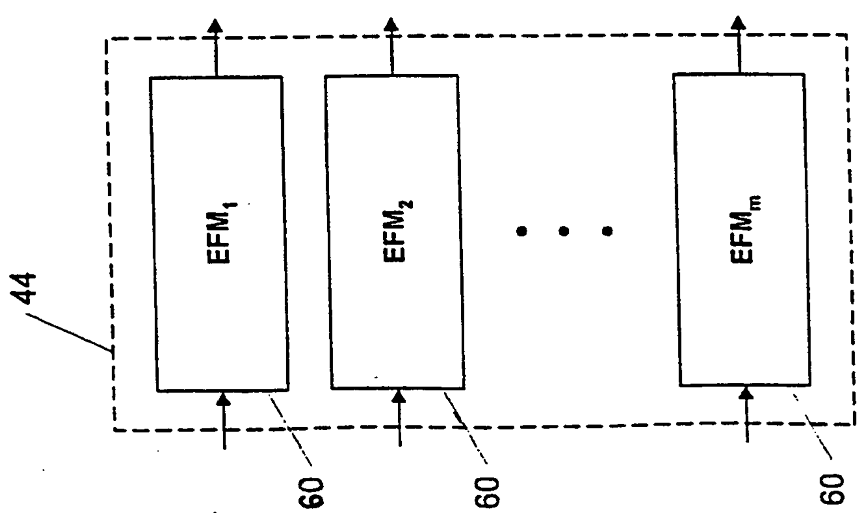

FIG. 5A

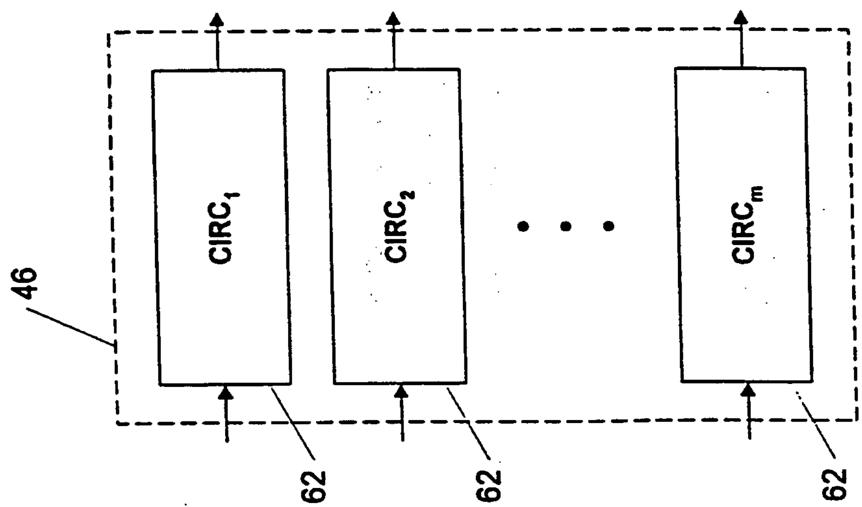

FIG. 5B

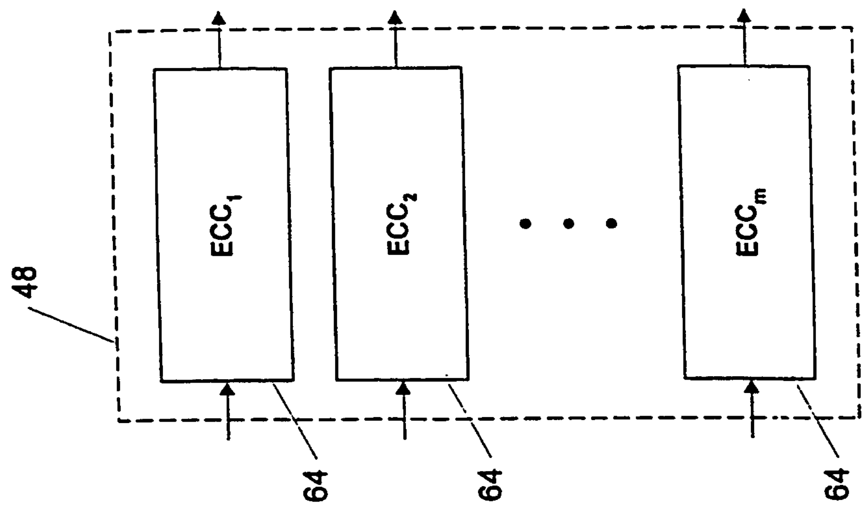

FIG. 5C

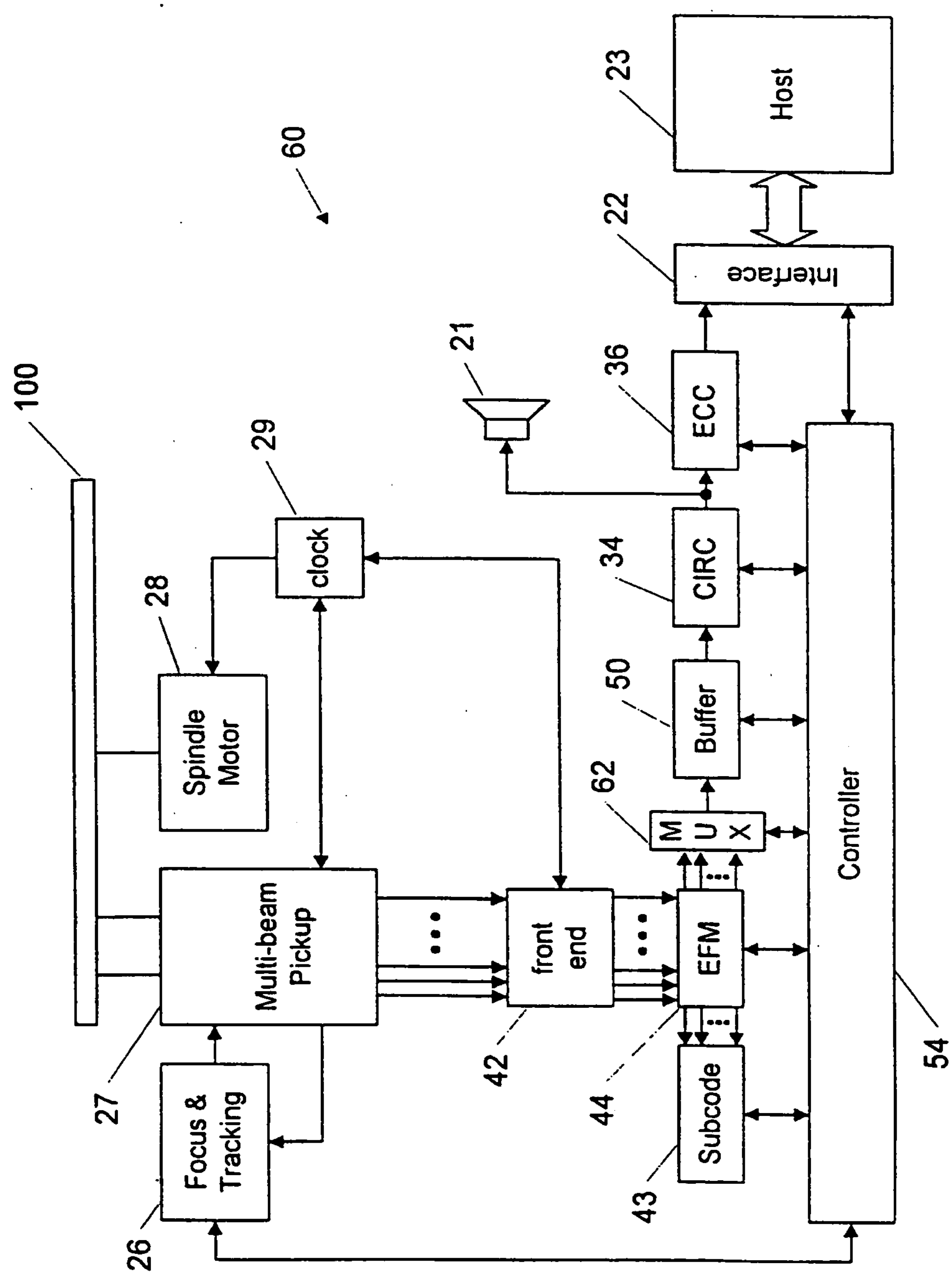
100
60
28
Spindle Motor
29
clock
27
Multi-beam Pickup
26
Focus & Tracking
42
front end
44
EFM
43
Subcode
62
MUX
50
Buffer
34
CIRC
36
ECC
21
22
Interface
23
Host
Controller
54

FIG. 6

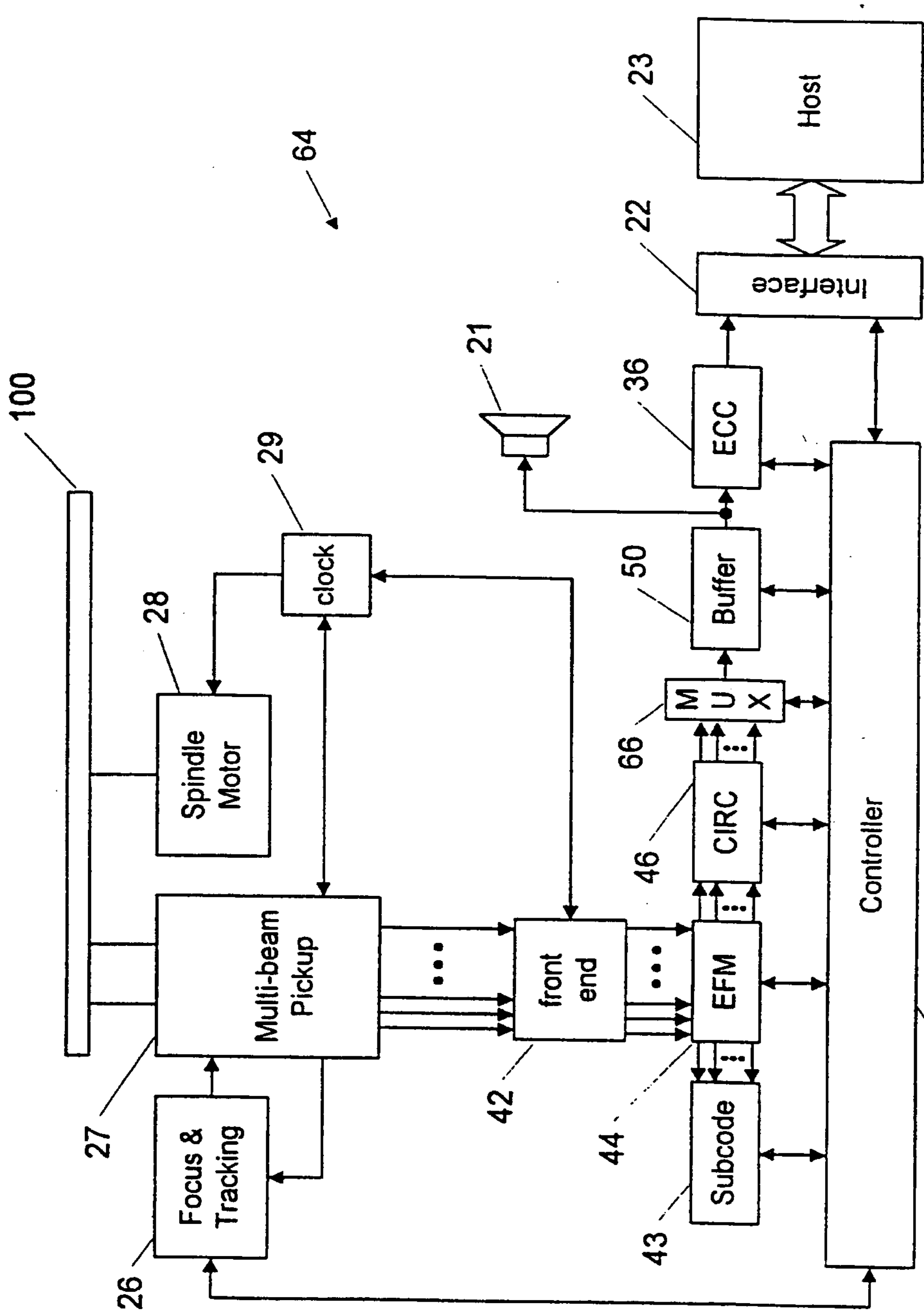
100
29
clock
28
Spindle Motor
Multi-beam Pickup
Focus & Tracking
27
26
front end
42
64
21
36
ECC
22
Interface
23
Host
50
Buffer
66
MUX
46
CIRC
EFM
44
Subcode
43
Controller
54

FIG. 7

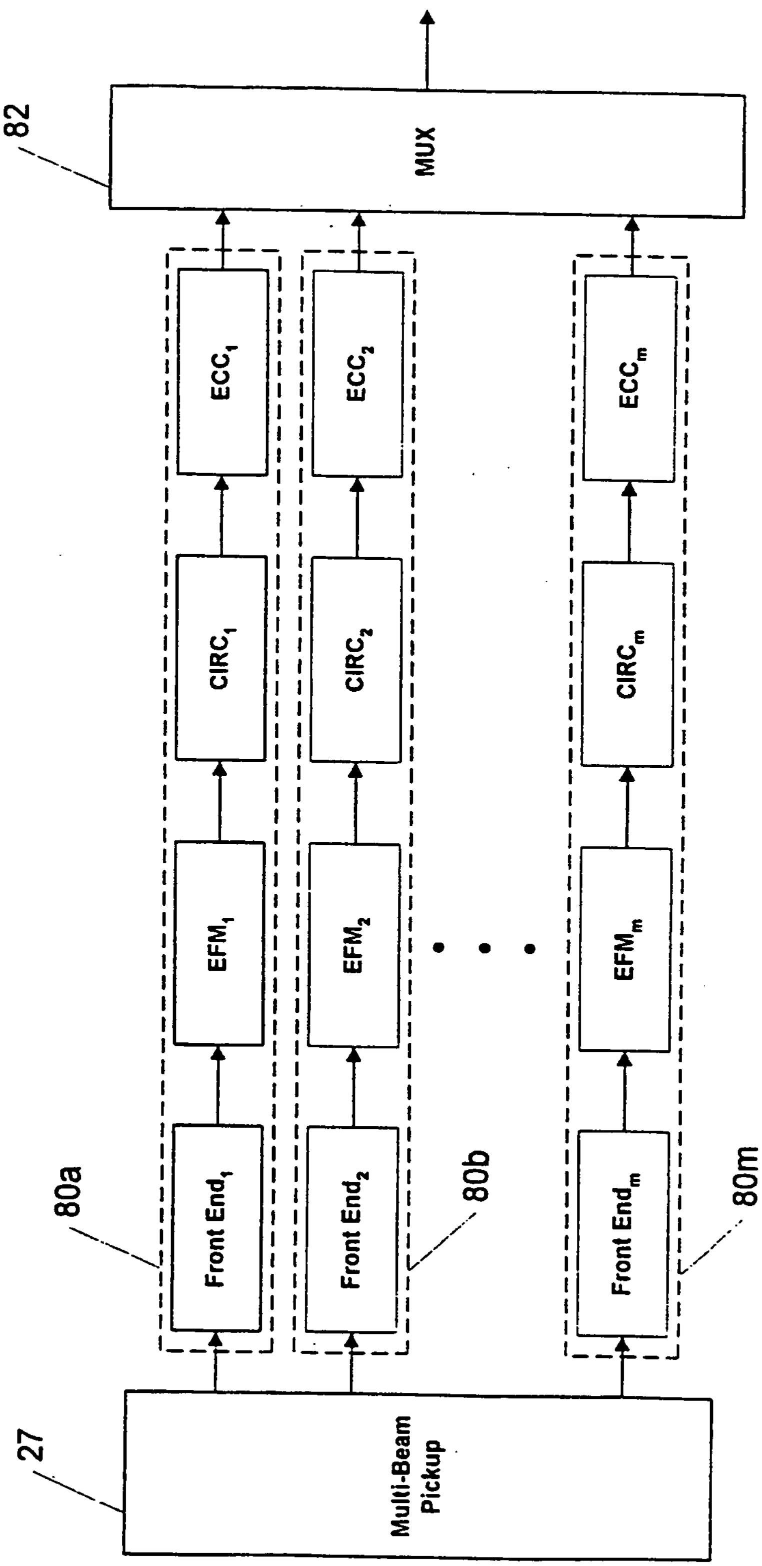
82
MUX
ECC_1
ECC_2
ECC_m
$CIRC_1$
$CIRC_2$
$CIRC_m$
EFM_1
EFM_2
EFM_m
Front End_1
Front End_2
Front End_m
80a
80b
80m
27
Multi-Beam Pickup

FIG. 8

INTERNATIONAL SEARCH REPORT

Int tional Application No
PCT/EP 98/00984

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 G11B7/14 G11B20/10

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 G11B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 0 643 388 A (MATSUSHITA ELECTRIC IND CO LTD) 15 March 1995	1-4,6-8, 12,13, 17,20, 21,24, 26-29
	see column 14, line 15 - column 15, line 52 see column 19, line 56 - column 20, line 52; figures 6,14,15	
Y		14,16,25
A		5,9-11, 18,19, 22,23

Y	US 5 347 506 A (MATSUDO YASUNORI ET AL) 13 September 1994 see abstract; figures 1,2	14,25
A		15

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
10 July 1998	17/07/1998

Name and mailing address of the ISA	Authorized officer
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1

Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

Inte ional Application No
PCT/EP 98/00984

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
Y	EP 0 714 096 A (SONY CORP) 29 May 1996 see abstract see column 3, line 18 - column 4, line 42; figures 1,2	16
X	EP 0 712 119 A (MATSUSHITA ELECTRIC IND CO LTD) 15 May 1996 see page 6, line 42 - page 7, line 5 see page 12, line 34 - line 55; figures 2,14	1,2,17, 26,27
A		3,15,18
X	EP 0 273 384 A (MATSUSHITA ELECTRIC IND CO LTD) 6 July 1988 see figure 7	1,2,12, 13,17, 24,26

1

INTERNATIONAL SEARCH REPORT

Information on patent family members

Inte ional Application No
PCT/EP 98/00984

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP 0643388 A	15-03-1995	JP 7078418 A	20-03-1995
		US 5506825 A	09-04-1996
US 5347506 A	13-09-1994	JP 5128532 A	25-05-1993
EP 0714096 A	29-05-1996	JP 8147897 A	07-06-1996
		CN 1126875 A	17-07-1996
		US 5590106 A	31-12-1996
EP 0712119 A	15-05-1996	JP 9167348 A	24-06-1997
EP 0273384 A	06-07-1988	JP 2583867 B	19-02-1997
		JP 63161532 A	05-07-1988
		JP 2583868 B	19-02-1997
		JP 63161533 A	05-07-1988
		JP 2084138 C	23-08-1996
		JP 7122962 B	25-12-1995
		JP 63161564 A	05-07-1988
		CA 1300261 A	05-05-1992
		US 4873679 A	10-10-1989

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(22) International Filing Date: 20 February 1998 (20.02.98)

(30) Priority Data:
08/804,105 20 February 1997 (20.02.97) US

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(74) Agent: VOSSIUS & PARTNER; Siebertstrasse 4, D-81675 München (DE).

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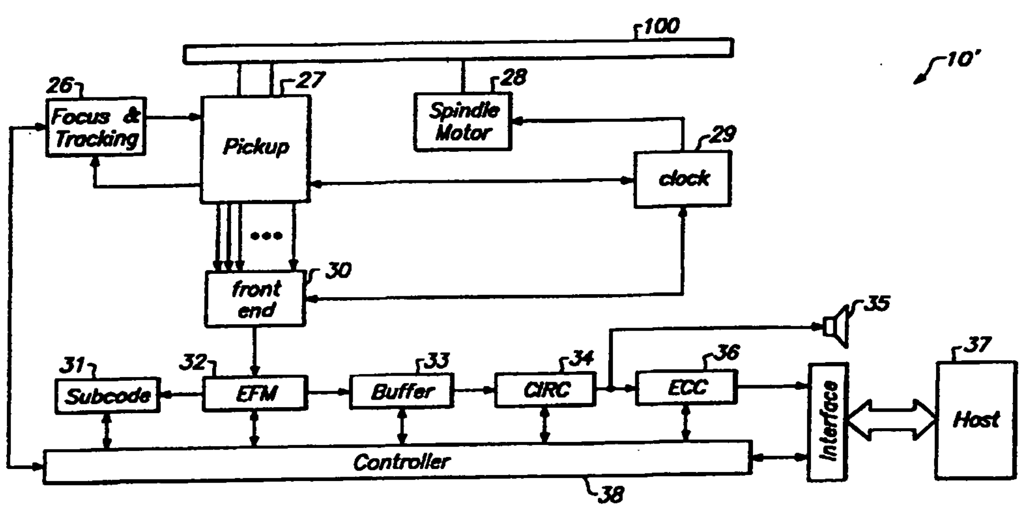
Published
Without international search report and to be republished upon receipt of that report.

(54) Title: METHODS AND APPARATUS FOR SYNCHRONOUSLY READING MULTIPLE TRACKS OF AN OPTICAL STORAGE MEDIUM USING MULTIPLE READING BEAMS



(57) Abstract

Methods and apparatus are provided for synchronously reading data from multiple tracks of an optical disk using multiple illumination beams. Circuitry is provided for use with a photodetector array to read and buffer data in parallel from the multiple adjacent tracks, while asynchronously providing processed data to a host processor. Circuitry is further provided for correcting phase errors resulting from variations in the linear velocity of the tracks being read, depending upon the radial position of the tracks.

METHODS AND APPARATUS FOR SYNCHRONOUSLY READING MULTIPLE TRACKS OF AN OPTICAL STORAGE MEDIUM USING MULTIPLE READING BEAMS

Field of the Invention

This invention relates to methods and apparatus for retrieving information from an optical disk at high data rates by simultaneously and synchronously reading multiple adjacent tracks.

Background of the Invention

Due to their high storage density, long data retention life, and relatively low cost, optical disks are becoming increasingly popular as a means to distribute information. Large format disks have been developed for storing full length motion pictures. The compact disk (CD), and more recent mini disk (MD) formats were developed and marketed for the distribution of musical recordings and have essentially replaced vinyl records. High-capacity, read-only data storage media, such as CD-ROM, have become prevalent in the personal computer field, while the new Digital Video Disk (DVD) format may soon replace videotape as the distribution medium for video information.

An optical disk is made of a transparent disk or substrate in which data, in the form of a serial bit-stream, is encoded as a series of pits in a

reflective surface within the disk. The pits are arranged along a spiral or circular track. Data is read from the optical disk by focusing a low power laser beam onto a track on the disk and detecting the light reflected from the surface of the disk. By rotating the optical disk, the light reflected from the surface of the disk is modulated by the pattern of the pits rotating into and out of the laser's field of illumination. Optical and imaging systems detect the modulated, reflected, laser light and produce an electrical signal which may be decoded to recover the digital data stored on the optical disk. The recovered digital data, which may include error correcting codes and additional subcoded information, is further processed to recover the stored data which may then be converted to audio signals, or used as executable programs and data depending on the type of optical disk being read.

To be able to retrieve data from anywhere on a optical disk, the optical systems include a pickup assembly which may be positioned to read data from any disk track. Servo mechanisms are provided for focusing the optical system and for keeping the pickup assembly positioned over the track, despite disk warpage or eccentricity.

Because in most previously known systems the data is retrieved from the disk serially, i.e. one bit at a time, the maximum data transfer rate for an optical disk reader is determined by the rate at which the pits pass by the pickup assembly. The linear density of the bits and the track pitch is fixed by the specification of the particular optical disk format.

For example, CD disks employ a track pitch of 1.6 μm, while the DVD employs a track pitch only about one-half as wide.

Previously known methods of increasing the data transfer rate of optical disk readers have focused on increasing the rate at which the pits pass by the pickup assembly by increasing the rotational speed of the disk itself. Currently, drives with rotational speeds of 2× to 10× standard speed are commercially available, and 12× designs are on the horizon. However higher disk rotational speeds place increasing demands on the optical and mechanical subsystems within the optical disk player, making such players more difficult and expensive to design and manufacture.

Other previously known techniques for increasing average data transfer rates involve methods to intelligently anticipate future read requests by a host processor. It has been observed that data access by computers frequently exhibit "locality of reference," which means that a future data access will be local, in either space or time, to a previous data access. Thus a CD-ROM drive or controller can "read ahead" and buffer the data that the host processor is likely to request next. When the host processor next requests data from the optical disk drive, the drive first checks if the requested data has already been read and buffered. If the data has already been buffered, the drive simply sends the buffered data to the host, avoiding the delays associated with repositioning the pickup assembly and reading data from the optical disk itself. While such caching techniques may speed up average data transfer rates, the maximum

data transfer rate is still limited by the rotational velocity of the optical disk within the optical disk reader.

U.S. Patent No. 5,627,805, incorporated herein by reference, describes a system to increase disk reading speeds by reading multiple tracks simultaneously. The data is read using a matrix detector that provides track signal data from each of a plurality of adjacent tracks. The system described therein employs a source of wide-area illumination to illuminate multiple tracks, which are then imaged onto the single matrix detector.

The present application is directed to an improvement in the system described in the above-incorporated patent, wherein the matrix detector and source of wide-area illumination are replaced by a multi-beam, multi-detector pickup assembly. Apparatus in accordance with the present invention obviates the Virtual Tracking System described in the foregoing application, instead employing conventional servo methods for tracking.

It would therefore be desirable to provide optical disk reading apparatus and methods that provide high speed retrieval of information from an optical disk while avoiding the limitations imposed on optical disk rotation speeds encountered by previously known devices.

It would also be desirable to provide an optical disk reading apparatus and methods that provide high speed retrieval of information from an optical disk using a multi-beam, multi-detector pickup assembly.

Summary of the Invention

In view of the foregoing, it is an object of the present invention to provide an optical disk reading apparatus and methods that provide high speed retrieval of information from an optical disk while avoiding the limitations imposed on optical disk rotation speeds encountered by previously known devices.

It is a further object of this invention to provide an optical disk reading apparatus and methods that provide high speed retrieval of information from an optical disk using a multi-beam, multi-detector pickup assembly.

These and other objectives of the invention are accomplished by providing methods and apparatus for processing, tracking, and reading data from multiple adjacent tracks simultaneously. In particular, apparatus constructed in accordance with the present invention employs a pickup assembly including a diffraction grating that splits a source of laser light into a plurality of beams for illuminating multiple tracks of an optical disk. A plurality of photodetectors simultaneously generate electrical data signals representative of the information-bearing pits on respective ones of the multiple adjacent data tracks of the optical disk. Methods and apparatus are provided for synchronizing the readout of the data from the multiple adjacent tracks to account for radial variations in linear velocity, and its effect on signal phase and frequency. Electrical data signals are then processed in accordance with previously known demodulation, decoding and error correction schemes and

the resulting bit stream is buffered. The buffered data is subsequently asynchronously read out of the buffer for further processing per se known in the fields of digital audio, video, and computer processing.

Further features of the invention, its nature and various advantages will be more apparent from the accompanying drawings and the following detailed description of the preferred embodiments.

Brief Description of the Drawings

FIG. 1 is an illustrative block diagram of a previously known optical disk reader;

FIG. 2 is an illustrative block diagram of an optical disk reader constructed in accordance with the principles of the present invention;

FIG. 3 is a block diagram of an illustrative embodiment of a multi-beam, multi-detector pickup assembly suitable for use in the present invention;

FIG. 4 is a detailed view of the arrangement of the detector elements in the pickup assembly of FIG. 3;

FIG. 5 is a block diagram of the front end circuitry for extracting data from the signals output by the pickup assembly of FIG. 3;

FIGS. 6A and 6B are more detailed block diagrams of the clock generation circuitry and exemplary frequency detector circuitry, respectively, of FIG. 5;

FIG. 7 is a block diagram of the data aligner and data sampler circuitry of FIG. 5;

FIG. 8 is a more detailed block diagram of exemplary data synchronization circuitry of FIG. 7;

FIG. 9A and 9B are, respectively, an alternative embodiment of the data aligner of FIG. 7 and a corresponding timing diagram;

FIG. 10 is yet another illustrative embodiment of the data aligner of FIG. 7; and

FIG. 11 is a flow chart outlining illustrative processes for reading a requested block of data from an optical disk and providing the requested block of data to a host processor.

Detailed Description of the Invention

By way of overview, a brief description of the components and operation of a previously known optical disk reader 10 is provided with respect to FIG. 1. The detailed description of the design and operation of such previously known optical disk readers may be found, for example, in Compact Disk Technology, H. Nakajima and H. Ogawa, published by Ohmsha, Ltd., Japan (1992), translated by Aschmann, C., IOS Press, Inc., Burke, Virginia, and The Compact Disk Handbook, Ken C. Pohlmann (2nd Ed. 1992), A-R Editions, Inc., Madison, Wisconsin, both of which are incorporated herein in their entirety by this reference. The present invention is then described where it differs in major respects from the previously known system of FIG. 1.

It will of course be understood that the prior art system of FIG. 1 is merely illustrative of the various types of optical disk apparatus in which the methods and apparatus of the present invention may be employed. Thus, for example, applicants expect that the invention described herein may be advantageously employed in any optical disk system, including DVD

systems.

Overview Of A Prior Art Optical Disk System

Illustrative previously known optical disk reader 10 comprises a spindle motor 11 that rotates optical disk 100 at high speed and pickup 12 including an illumination source and a photodetector for generating electrical signals representative of information-bearing pits formed in a reflective surface within optical disk 100. The electrical signals from the photodetector of pickup 12 are then passed to front end circuitry 13 for extracting a digital data signal. Under the control of controller 24, the data signal is further processed by eight-to-fourteen (EFM) demodulation circuitry 17, Cross Interleaved Reed-Solomon Code (CIRC) circuitry 18, error correction code (ECC) circuitry 19, and subcode circuitry 16. Controller 24 also controls focus and tracking circuitry 14, as well as buffer 20 and interface 22.

For a digital audio system, the data signals may be processed into suitable analog signals (using circuitry not shown) connected to audio means 21. Similarly, if the optical disk contains video images, the data signals may be processed for direct display on a TV or monitor. In computer applications the data signals are typically transferred from buffer 20 to host processor 23 via interface 22.

Spindle motor 11 spins optical disk 100 at a speed that depends upon the radial location of pickup assembly 12 (for example, for a 1× CD-ROM spindle speed, approximately 200-500 RPM), to maintain a constant linear velocity of an optical disk track relative to pickup assembly 12. For a CD-ROM format,

this linear velocity is generally 1.4 m/s, while for the DVD format it approaches 4 m/s. Pickup assembly 12 typically includes a laser diode that illuminates only a single data track on optical disk 100 and an optical sensor onto which an image reflected from the optical disk is projected. The intensity, or other property, of the light beam reflected from the surface of optical disk 100 is modulated by inhomogeneities in the reflective surface of the optical disk (i.e., bumps or pits, referred to hereinafter as "data spots") arranged in spiral or circular tracks on optical disk 100.

Pickup assembly 12 includes circuitry to generate an electronic signal representative of the modulation in the illumination impinging upon its optical sensor due to the presence of the data spots. To ensure that the laser illumination remains focused on the reflective surface of optical disk 100, pickup assembly 12 also provides signals to focus and tracking subsystem 14.

The data spots are recorded on optical disk 100 using a modulation code that permits a data clock to be recovered from the data as it is read off of the optical disk. Clock circuitry 15 includes phase-locked-loop (PLL) circuitry for recovering the data clock from, and maintaining the data clock in synchrony with, the modulated electronic signal from pickup assembly 12. In addition to being used for extracting the data from the modulated signal, the data clock is representative of the linear velocity of the data track relative to pickup assembly 12 and may be used as a feedback signal to control the speed of spindle motor 11 to maintain a constant linear velocity.

Front end circuitry 13 uses the data clock from PLL 15 to recover a serial stream of bits from the electronic signal. Front end circuitry 13 contains additional circuitry to identify synchronization codes in the bit stream so that the serial bit stream may be correctly assembled into multi-bit data words which are transferred to demodulation circuitry 17. Demodulation circuitry 17 may be programmed for eight-to-fourteen demodulation, eight-to-fifteen demodulation (as in the SD systems), eight-to sixteen demodulation (EFM Plus), or may use another suitable demodulation scheme. The demodulated data words, or symbols, are then assembled into blocks and decoded by CIRC decoder 18 using a form of Cross Interleaved Read-Solomon code, for example, CIRC for CD-formats and CIRC Plus for DVD. Demodulated data words are also provided to subcode processor 16 which extracts data, such as block numbers, or song titles, that may be recorded in the subcode channels embedded in each block of data words.

For video and audio optical disk players, the data from CIRC decoder 18 represents, in digital form, the video or audio signal that was originally recorded and stored on the disk. These signals may then be converted to analog signals and the original recorded signal reproduced using conventional audio or video devices 21. Errors in the recovered audio or video signals are handled by interpolation and filtering circuitry (not shown) to calculate a value to use in place of the erroneous data. Because of the interpolation process, isolated errors in an audio or video signal are unlikely to be noticed when listening to the audio or viewing the video signals.

However, since a single bit error in data representing a computer program may render the program inoperable or the data unusable, optical disks used for the storage and distribution of data and programs must have very low data error rates. To reduce the data error rates to acceptably low levels, error correction codes (ECC) are added to the data when it is recorded to the disk. ECC circuitry 19 uses error correcting codes to detect and possibly correct errors in the data. Finally, the data is buffered in memory buffer 20 for transfer to host processor 23 via interface circuitry 22. Controller 24 coordinates operation of each of the optical disk reader subsystems and to control the operation of the optical disk reader as a whole.

In the previously known optical disk reader of FIG. 1, the rate of data transfer between the optical disk itself and the host processor is limited by the rate at which the data can be processed by the circuitries shown in FIG. 1. For example, for a 1× CD-ROM reader, the data rate of the signal being read from the optical disk is about 4.32 MHZ, well within the processing capabilities of the electronic circuits involved. Even in optical disk readers having a spindle speed 8× the standard speed, the data transfer rate is limited by the speed at which the data can be read off the disk.

Overview Of The Present Invention

Referring now to FIG. 2, optical disk reader 25 is described that provides a high data transfer rate, in accordance with the principles of the present

invention, by reading multiple tracks of data from an optical disk simultaneously. Much of the circuitry of FIG. 2 may be common to or readily adapted from the circuitry of the system of FIG. 1. Accordingly, the following description describes in detail the differences between a previously known optical disk reader and apparatus 25 constructed in accordance with the principles of the present invention.

In particular, apparatus 25 includes a multi-beam, multi-detector pickup assembly for illuminating and reading multiple adjacent data tracks; phase-lock loop circuitry that permits a clock associated with a reference track to be used for synchronizing the recovery of data from neighboring tracks; and a parallel write/asynchronous read architecture that enables blocks of data to be read from the optical disk, processed and written to a buffer in parallel while being asynchronously retrieved from the buffer by a host computer.

Apparatus 25 of FIG. 2 includes pickup assembly 27 including a source of laser illumination, a diffraction grating for splitting the laser illumination into three or more illumination beams and a corresponding number of photodetectors onto which multiple illumination beams, reflected from the optical disk, are focused by an optical system. Pickup assembly 27 is described in greater detail hereinbelow. Each of the multiple photodetectors in pickup assembly 27 generates an electrical signal representing data read from a corresponding data track on optical disk 100, and provides that electrical signal to front end circuitry 30.

Front end circuitry 30 performs a function similar to that of front end circuitry 13 of FIG. 1, except that multiple bit streams are processed concurrently, so additional circuitry is provided for buffering and synchronizing data transfers to subsequent processing circuitry. Front end circuitry 30 also includes a multiplexer for routing multiple data streams to demodulation circuitry 32.

Memory 33 is provided to buffer the data read from the multiple data tracks, and to decouple the process of reading data from optical disk 100 from the process of transferring the data to host processor 37. Memory 33 therefor is large enough to hold about as many data blocks from multiple data tracks of optical disk 100 as can be read in one revolution of optical disk 100. Controller 38 maps data from the multiple data tracks to memory 33 so that individual data blocks will be correctly assembled without overwriting one another. As will be appreciated by those of skill in the art of buffer design, this mapping may be either dynamic or static.

With respect to FIG. 3, pickup assembly 40 suitable for use in an optical disk reader constructed in accordance with the principles of the present invention is described. Pickup assembly 40 includes source of laser illumination 41, i.e., a laser diode, diffraction grating 42, beam splitter 43, objective lens 44, and photodetector array 46. Diffraction grating 42 splits the laser light emitted by laser diode 41 into three (or more) illumination beams, which are bent by beam splitter 43 and focused by objective lens 44 onto three (or more) adjacent tracks of

information-bearing pits on optical disk 100. As will of course be understood, the illumination beams are spaced apart by the track pitch, for example, for the CD-ROM format, 1.6μm apart. The illumination beams, once reflected from the information bearing surface within optical disk 100, pass through beam splitter 43 and are focused on corresponding photodetectors in photodetector array 46. Alternatively, multiple beams may be formed from the light emitted by the laser diode using the beam splitter apparatus described, for example, in Corsover et al. U.S. Patent 4,459,690.

As shown in FIG. 4, photodetector array 46 includes a central four quadrant detector comprising elements 46a-46d, and outboard detectors 46e and 46f for reading adjacent data tracks. Photodetector array 46 illustratively includes three detectors for reading three adjacent tracks of optical disk 100, although additional detectors may be disposed on either or both sides of the four quadrant detector (indicated by dotted line detector elements g and h).

Detectors 46a to 46d are summed to provide an electrical signal representative of the information contained in the data track imaged onto the four quadrant detector by the optical system, while detectors 46e and 46f provide electrical signals representative of the information contained in the adjacent data track on either side of the track imaged onto the four quadrant detector. As is conventional, the difference between the sums of the diagonal quadrants, i.e., e_{focus} = (46a+46d)-(46b+46c), may be computed to generate a focus signal using the well known astigmatism method, while a tracking signal may

be generated as the difference of the sums of the quadrants on the same side of the track, i.e., $e_{track} = (46a+46c)-(46b+46d)$. The focus error signal e_{focus} and tracking error signal e_{track} are input to focus and tracking circuitry 26.

Multi-track Phase Lock Loop Circuitry

Referring now to FIG. 5, pickup assembly 27 outputs track data signal, $T_1 \ldots T_m$, corresponding to **m** tracks being read (illustratively, three for the pickup assembly of FIGS. 3 and 4). The track data signals, $T_1 \ldots T_m$, output by photodetector array 46 are then processed by front end circuitry 30, including clock generating circuitry 50 and track processing circuitry 51, to extract data from each track signal. Multiplexer 54 selects extracted data words from each of track processing circuitries 51 for decoding by eight-to-fourteen decoder 32.

An accurate data clock is needed to reliably extract the data from the track data signals. By design, a track data signal is self-clocking, that is, the data stored in a data track is formatted so that a data clock can be recovered from the track signal. Typically, a Phase-Locked Loop (PLL) is used to recover the clock signal from the track data signal. In optical disk reader 25 of the present invention, clock generation circuitry 50 recovers a reference clock signal from a selected one of the multiple data tracks being read. The reference track may be, for example, the middle, innermost or outermost track of the multiple tracks being read.

The reference clock, Φ_{REF}, generated by clock generation circuitry 50 has a frequency and phase which

are correct for the reference track data signal. However, because the track data signals are read from tracks having different radii, and therefore slightly different linear velocities, the corresponding track data signals differ slightly in frequency and may differ substantially in phase. For example, for a CD-ROM optical disk, applicants have determined that the change in linear velocity, and therefore the difference in track data signal frequency, between any two adjacent tracks is approximately 0.01% anywhere on the optical disk. Furthermore, since the track data signal frequencies differ, the phase difference between any pair of tracks varies continuously. Consequently, a single data clock cannot be used directly to extract data from each track data signal. Front end circuitries 51 therefore include data aligner circuitry 52, for synchronizing reference data clock Φ_{REF} to the individual track data signals, and data sampler circuitry 53, for sampling the track data signal.

Front end circuitry 51 also includes first-in/first-out buffer (FIFO) 49 for assembling the serial data into parallel data words and for synchronizing transfer of the assembled data words from front end circuitry 51 to EFM circuitry 38 via multiplexer 54. Advantageously, assembling the data words in front end circuitry 41 reduces the frequency at which subsequent circuitry operates. For example, in a standard speed CD-ROM drive, each track has a data rate of approximately four million bits per second (Mbps). Thus, multiplexer 54 would have to operate at a frequency of approximately 40 MHz (4 Mbps × 10 tracks).

However, by converting the data into words reduces operating frequency to about 2.9 MHz (40 Mbps/14 bits per word), greatly simplifying circuit design.

Referring now to FIGS. 6A and 6B, clock generation circuitry 50, is described in greater detail. The core of clock generation circuitry 50 is formed by accumulator 55, comprising full adder 56 and register 57. The output of register 57 is fed back to one of the inputs of full adder 56; the other input being a frequency increment value supplied by filter 59. Register 57 latches the output of full adder 56 on every cycle of on its clock input. Since the output of full adder 56 is the sum of the contents of register 57 and the frequency increment, the data value stored in register 57 is incremented by the frequency increment every clock cycle.

The clock input to register 57 is provided by a radio frequency (RF) clock signal Φ_{RF}. Although many frequencies may be used, frequencies greater than about 200 MHZ are preferable, as higher frequencies provide greater precision and finer control over the frequency of reference clock, Φ_{REF}.. Thus, the data value in register 57 is incremented at a rate determined by the frequency increment provided by filter 59 and the frequency of Φ_{RF}.

Eventually, the sum of the frequency increment and the value stored in register 57 will no longer fit in register 57, and the register will overflow. A new clock signal, Φ_{REF}, may then be generated whenever register 57 overflows, which will occur at a frequency given by:

$$F_{REF} \approx F_{RF}\left(\frac{\mathit{Frequency\ Increment}}{\mathit{Register\ Capacity}}\right) \approx F_{RF}\left(\frac{\mathit{Frequency\ Increment}}{2^{\mathit{Register\ size}}}\right) \quad (1)$$

Alternatively, the most significant bit (MSB) of register 57 may provide the new clock signal. While the frequency of Φ_{RF} and the size of register 57 are fixed, the value of the frequency increment may be generated so that the frequency of Φ_{REF} is a multiple of the bit rate of reference track T_{REF}, e.g., eight times the bit rate.

Although the nominal bit rate of a CD-ROM is known, the CD-ROM specification permits a variation of ±10% in linear track velocity. Thus, the bit rate of the reference track may also vary. In accordance with the principles of the present invention, frequency detector 58 varies the frequency increment as needed to adjust Φ_{REF} to match the T_{REF} bit rate.

Data on a CD-ROM is encoded using an eight-to-fourteen code, in which no fewer than three and no more than eleven consecutive bits have the same value. Since data is recorded so that the beginning and end of a data spot indicate transitions in the bit pattern (i.e., 0 to 1 or 1 to 0), a track data signal appears as a square wave in which the positive and negative half cycles are at least three, and at most eleven, bit periods long. Thus, in accordance with principles of the present invention, a proper data clock frequency can be determined by measuring the pulse width of the longest and/or shortest positive and negative half cycles in a track data signal. By extension, other unique pulse widths, such as the shortest possible

pulse width, or the duration of a unique sequence of pulses, may be used.

Advantageously, data on a CD-ROM is organized into sectors and frames, wherein each frame is 588 bit periods in length and begins with a unique synchronization pattern comprising a sequence of eleven identical bits of one polarity followed by eleven bits of the opposite polarity (e.g., 0000000000011111111111 or its complement), otherwise referred to herein as an (11,11) pattern. Thus, once every 588 data clock periods a data track signal should contain a pulse width of eleven clock periods.

Referring now to FIG. 6B, frequency detector 58 includes two counters, positive pulse width counter 61 and negative pulse width counter 62. Positive pulse width counter 61 is reset during a negative half-cycle of the reference track data signal. During a positive half cycle, positive pulse width counter 61 measures the width of the half-cycle by counting cycles of clock Φ_{REF}. Similarly, negative pulse width counter 62 measures the width of negative half-cycles of the reference track data signal. Divide by "n" block 60 may be provided to alter the resolution of the counters by altering the rate the counters are clocked.

Maximum tracking circuitries 63 and 64 keep track of the largest count reached by pulse width counters 61 and 62, respectively, during a search interval or window. Maximum selecting circuitry 65 then selects the larger of the outputs of maximum tracking circuitries 63 and 64 for use in calculating a new frequency increment by block 67.

Search window counter 66 is configured to

periodically reset maximum tracking circuitries 63 and 64, and maximum selecting circuitry 65. Because each frame of data begins with an (11,11) pattern, frequency detector 58 should see an eleven-bit-wide pulse at least once a frame. Therefore, search window counter 66 should not reset the other circuits more often than once per data frame. For example, search window counter 66 may reset the maximum tracking and selecting circuitries 63-65 at most once every 512 data clock cycles, and preferably about every 600 data clock cycles.

As noted above, the maximum pulse width should be eleven bit periods wide. A pulse width more than eleven bit periods wide indicates that the reference clock frequency is to high, and should be reduced. Conversely, a shorter pulse width indicates a reference clock frequency that is too low. From equation (1), the reference clock frequency is directly proportional to the frequency increment, thus, the reference clock frequency may be raised by using a larger frequency increment. Although many functions may be used to calculate a new frequency increment, a suitable function for this purpose is given by:

$$(\mathit{Freq.\ Increment})_{new} = (\mathit{Freq.\ Increment})_{old} \times \frac{11\,\mathit{bit\ periods}}{\mathit{Max\ pulse\ width}} \quad (2)$$

wherein *max pulse width* refers to the length of an 11-bit pattern as measured by counters 61 or 62; and 11 *bit periods* refers to the correct length.

At times, large changes in the reference clock frequency may be undesirable. For example, when

trying to lock onto the frequency of the reference track data signal after repositioning pickup 27 (FIG. 2), large changes in reference frequency may be acceptable. However, after frequency lock occurs and data is being read from multiple data tracks on the disk, sudden large changes in the reference clock frequency may cause data errors. Accordingly, the frequency increment is preferably filtered to provide a controlled transition from the old value to the new value.

For example, the frequency increment may be filtered using Equation **(3)**. In Equation **(3)**, the new frequency increment is a weighted average of the old

$$FI_{new} = (1-\alpha)\, FI_{calculated} + (\alpha)\, FI_{old} \qquad \textbf{(3)}$$

frequency increment and the frequency increment calculated from Equation **(2)**, wherein the relative contributions of the old and calculated values is determined by the value of α. Thus, the size of any change in the reference clock frequency by appropriate selection of α. For example, small values of α enable large, rapid frequency changes so a new frequency may be acquired rapidly, whereas large values of α may be used to limit frequency changes after frequency lock is obtained. Preferably, α is a power of 2, so that Equation **(3)** may be calculated using simple shift and add operations.

Referring to FIG. 7, data aligner circuitry 52 of front end circuitry 30 uses reference clock signal Φ_{REF} to generate track data clocks, Φ_{TRACK}, synchronized to each track being read. Front end

circuitry 30 also includes data sampler 53 which uses a corresponding Φ_{TRACK} to sample the track data signals T_1-T_m at the center of each bit period.

Reference clock signal Φ_{REF} is used as the clock input to shift register 70, which is configured as a ring counter. Shift register 70 is loaded with a bit pattern having only a single bit which is set, for example 01000000_2, the remaining bits being cleared. Each pulse of reference clock Φ_{REF} causes the bit pattern in shift register 70 to shift one bit position, or cell. A bit which is shifted out the end of shift register 70 is "wrapped around" and shifted back in at the other end of the shift register. Thus the single set bit in shift register 70 circulates through each cell in the register at a rate determined by reference clock Φ_{REF}.

The value of each cell in shift register 70 is input to multiplexer 71, which functions to output the value of a selected one of the shift register cells. The combination of shift register 70 and multiplexer 71 functions to divide the frequency of reference clock Φ_{REF} by the number of bits in the shift register to produce track data clock Φ_{TRACK}. For example, if shift register 70 were to have eight bits, each bit position would have a '1' bit in it only once every eight pulses of the reference clock. Thus if multiplexer 71 were to selectively output the value of bit three of shift register 70, the output of the multiplexer would be a '1' whenever there was a '1' in bit position three of the shift register, i.e. once every eight pulses of reference clock Φ_{REF}.

Ideally, the phase of the track data clock

Φ_{TRACK}, should be such that the track data signal, T_n, is sampled at the center of each bit period. If the track data clock phase is not correct, the track data signal may be sampled too early or too late in each bit period, thereby risking sampling the data track signal during a transition from one bit to the next. Phase detector 73 measures the relative phase between track data clock Φ_{TRACK} and track data signal T_n and provides an error signal indicative of the phase error to error accumulator 74.

Filter 75 smooths the accumulated phase error values to remove clock jitter and small variations in phase error. The output of filter 75 is used by select logic 72 to control multiplexer 71 to reduce any phase error. When the error is sufficiently large to warrant corrective action, selector 72 adjusts the phase of track clock Φ_{TRACK} by causing multiplexer 71 to select a different input to pass through to its output. Changing the input of multiplexer 71 either inserts or removes a small amount of time to the interval from one track clock pulse to the next such pulse. For example, if shift register 70 has eight bits and is designed to shift bits to the right, and if selector 72 causes multiplexer 71 to change its input one bit position to the left, the next pulse output by multiplexer 71 will occur on the seventh reference clock pulse instead of the eighth. Conversely, changing the input of multiplexer 71 one bit position to the right will cause a track clock pulse to occur on the ninth reference clock pulse. Thus by changing the bit selected by multiplexer 71, the phase and frequency differences between the reference track data signal and another

track data signal can be corrected.

Because a track clock pulse cannot be dropped or missed without corrupting the recovered data, selector 72 includes logic to prevent selection of a different input by the multiplexer at an inopportune time. For example, if multiplexer 71 is reading bit position 6 of shift register 70, a '1' is in bit position five, and shift register 70 shifts right (i.e. the '1' in bit position six moves to bit position five) at the same instant selector 72 switches the input of multiplexer 71 from bit position five to bit position six, a clock pulse will be missed, and a data bit will not be sampled correctly. Just as a change in input to multiplexer 71 in a direction opposite to the direction of the bit shifts in shift register 70 can cause a dropped clock pulse, a change in the same direction as the bit shifts can cause an extra clock pulse to occur. Since too few or too many clock pulses may garble the data being read, selector 72 monitors the output of shift register 70 to avoid the occurrence of situations which may lead to data corruption.

A more detailed illustrative embodiment of data aligner and data sampler circuitry 51 of FIG. 7 is described with respect to FIG. 8. Edge detector 80 comprises flip-flops 81a and 81b, and XOR gate 82. Flip-flops 81a and 81b are configured as a shift register having an input connected to the track data signal T_n and clocked by reference clock, Φ_{REF}. XOR gate 82 compares the values of the two flip-flops and provides an edge signal whenever the outputs of the flip-flops differ, thus indicating an edge in the track data signal. The edge signal is latched by flip-flop

83a. Flip-flop 83b holds the previous value of the edge signal.

Phase detector 73, including up-counter 84, down-counter 85, and latch 86, determines the phase relationship between the occurrence of pulses of the track data clock, Φ_{TRACK}, output by multiplexer 71 and edges in the track data signal as determined by edge detector 80. Ideally, a signal from edge detector 80 should occur midway between successive pulse of track data clock Φ_{TRACK}. An edge signal which occurs early indicates that track clock Φ_{TRACK} is slow, and conversely a late edge pulse indicates the track clock is fast.

Up-counter 84 is reset by the track data clock, and begins counting up at a rate determined by reference clock Φ_{REF}. When an edge is detected by edge detector 80, the output of up-counter 84 is loaded into down-counter 85, which counts down at the same rate as up-counter 84. On a subsequent track clock pulse, the value of down counter 85 is latched by latch 86. If the edge occurred midway between successive track data clocks, the time spent counting up equals the time spent counting down and the value in latch 86 should be zero. However, if the edge occurs early, more time is spent counting down and a negative value is latched. Conversely, a positive value indicated a late edge detection.

The output of phase detector 73 indicates the position of an edge pulse relative to the midpoint between successive track clock pulses, and, therefore, represents a phase error in the track data clock. The phase error is accumulated by latch 87a and adder 88a, and subsequently filtered by adder 88b and latch 87b to

produce an average error level. Note that it may be necessary to sign extend the output of phase detector 73, to avoid underflow and overflow conditions in adders 88a and 88b. As described herein above, the average, filtered, phase error signal is then used by select logic 72 to control multiplexer 71 and thereby adjust the track data clock phase and frequency as needed to minimize the average phase error.

In FIG. 9A, alternative data aligner 90 is shown. As discussed hereinabove, reference clock Φ_{REF} is derived from the reference track data signal. Since it has a frequency that is a multiple of the reference track data frequency, an interval corresponding to bit period in the track data signal may be measured by counting cycles of Φ_{REF}. The ratio of Φ_{REF} to the reference track data rate is referred to herein as the over sampling factor.

Data aligner 90 includes edge detector 91, which may be the same as edge detector 80 of FIG. 7, as well as counters 92 and 93. When an edge is detected in the track data signal by edge detector 91, counter 92 is reloaded with a value equal to half the over sampling factor and begins counting down at a rate determined by Φ_{REF}. When counter 92 reaches zero the track data signal is sampled and the counter stops counting. Since the initial count in counter 92 was half the over sampling factor, the track data signal is sampled approximately in the middle of the first bit period following the detected edge.

In addition, when counter 92 reaches zero, counter 93 is loaded with a value equal to the over sampling factor and begins to count down. Thus, counter 93 measures a one bit period interval beginning

half a bit period after an edge in the track data signal. When counter 93 subsequently reaches zero, the track data signal is sampled. However, unlike counter 92, counter 93 repeatedly reloads and counts down, so that the track data signal is sampled at successive bit periods.

The operation of data aligner 52 of FIG. 9A may be more clearly understood by considering the timing diagram of FIG. 9B. Wherein edge 94a causes counter 92 to reload and begin counting down. Counter 92 reaches zero and outputs signal 95a near the mid point of bit period 96a. This signal reloads counter 93 and also causes the track data signal to be sampled. Counter 93 then reaches a zero count and outputs signal 97a causing the track data signal to be sampled near the mid point of bit period 96b. Counter 93 repeats its countdown, thus, sampling successive bits in the track data signal until reset by counter 92 following edge 94b. Also shown is an exemplary decoding of the track data signal of FIG. 9B.

A somewhat simpler embodiment of the data aligner is shown in FIG. 10. Data aligner 101 includes synchronous finite state machine (FSM) 102 having a number of states equal to the over clocking factor. An exemplary state transition table for an eight state FSM is shown below.

Absent a signal from edge detector 103, FSM 102 cycles to the next state on each cycle of Φ_{REF}. When state `0' is reached, a signal is output causing the track data signal to be sampled at fixed intervals equal to one bit period. However, when an edge has been detected, FSM 102 transitions to a middle state, e.g., state four, such that state `0' will be reached, and the track data signal sampled, half a bit period

following the detected edge. Thus, the occurrence of an edge in the track data signal re-synchronizes FSM 102 with the track data signal so that data sampling occurs near the mid point of each bit period.

Parallel Write/Asynchronous Read Buffer

Referring now to FIGS. 2 and 11, illustrative processes for reading and writing blocks of data in parallel from the optical disk to a buffer and for reading a block of data requested by host processor 37 are described. The process of providing a data block to a host processor is split into two asynchronous processes illustrated by flowcharts 110 and 210, corresponding, respectively, to reading data from the disk and the process of providing the data to the host processor.

Process 110 is entered, at 112, with a request to read a total of **k** data blocks starting at block **n**. At steps 114 and 116, controller 38 (see FIG. 2) calculates, or looks up in a table, the track **t** which contains data block **n**, and, if required, positions pickup assembly 27 to read track **t** as well as its adjacent tracks. When the pickup assembly has settled, a desired number of data blocks are read in parallel from optical disk 100 and stored in buffer 33. As data blocks are written to buffer 33, a Block Address Table is updated to reflect the block numbers currently stored in the buffer. If at step 120 it is determined that all **k** data blocks have not been read, a new starting block is determined (step 124), and the pickup assembly is repositioned (step 122). Data reading process 110 terminates when all of the

requested data has been read and transferred to buffer 33.

The process of flowchart 210 is performed concurrently with the process of flowchart 110. This process is entered when the host processor requests **k** data blocks beginning at block **n**. Upon receiving this request, controller 38 first determines at block 216 whether the data block is already in buffer 33 by consulting the Block Address Table. If the data block is present, then the data block is retrieved from buffer 33 and transferred to host processor 37. If the data block has not been read yet, the process of flowchart 110 is initiated to read the desired block while process 210 waits for the data to become available in buffer 33. These steps are repeated as necessary until the last block of the requested data has been transferred to the host processor.

In process 210, when a desired data block is read from buffer 33, the pointer to that portion of buffer 33 may be freed to be subsequently written by the blocks of data being read off of the optical disk by process 110. As described hereinabove, in one preferred embodiment of the invention, buffer 33 is capable of holding the data for about one full revolution of optical disk 100, e.g., buffer 33 is at least large enough to hold the data in one revolution of a single track multiplied by the number of tracks being read in parallel.

While preferred illustrative embodiments of the present invention are described, it will be obvious to one skilled in the art that various changes and modifications may be made therein without departing

from the invention and it is intended in the appended claims to cover all such changes and modifications which fall within the true spirit and scope of the invention.

What Is Claimed Is:

1. Apparatus for simultaneously reading first and second data tracks of an optical disk, the apparatus comprising:

a pickup assembly providing first and second data signals corresponding to data stored in the first and second data tracks;

sampling circuitry for recovering first and second digital data signals from the first and second data signals; and

synchronizing circuitry for synchronizing the sampling circuitry to account for variations in the linear velocities of the first and second data tracks.

2. Apparatus as defined in claim 1 wherein the synchronizing circuitry comprises circuitry for providing a reference clock signal based on the first data signal and circuitry for generating a track data clock signal from the reference clock signal, wherein the track data clock signal has a phase and frequency suitable for sampling the second data signal.

3. Apparatus as defined in claim 2 wherein the synchronizing circuitry comprises a digital phase locked loop.

4. Apparatus as defined in claim 2 wherein the first data signal comprises a plurality of pulses, at least one of the plurality of pulses having a unique pulse width, the synchronizing circuit comprising:

measuring circuitry for measuring the width of each of the plurality of pulses;

timing circuitry for measuring a time period;

identifying circuitry, coupled to the measuring circuitry and timing circuitry, for identifying the occurrence of a pulse having the unique pulse width during the time period; and

calculation circuitry for calculating a desired frequency of the reference clock signal from the measured pulse width of the pulse having the unique pulse width.

5. Apparatus as defined in claim 4 wherein the synchronizing circuitry further comprises:

a ring shift register coupled to the reference clock signal;

a selector coupled to the shift register for generating the track data clock signal from the reference clock signal;

an edge detector coupled to the reference clock signal and to the second data signal, the edge detector detecting an edge in the second data signal;

a phase detector coupled to the reference clock signal, the track data clock signal, and the edge detector, the phase detector determining a timing relationship between the track data clock signal and an edge in the second data signal; and

an error accumulator coupled to the phase detector and the selector, for controlling the selector to adjust the track data clock signal responsive to the timing relationship.

6. Apparatus as defined in claim 2 wherein the circuitry for generating the track data clock

signal comprises:

circuitry for generating track data clock pulses, wherein successive track data clock pulses are separated by a number of intervals each having a duration related to a period of the reference clock signal;

circuitry for determining a timing relationship between an edge in a selected one of the data signals and a preceding and succeeding pulse in the corresponding track data clock signal; and

circuitry for adjusting the number of intervals between successive pulses of the track data clock responsive to the determined timing relationship.

7. Apparatus as defined in claim 6 wherein the circuitry for adjusting comprises:

circuitry for generating an error signal indicative of the determined timing relationship;

circuitry for filtering the error signal; and

circuitry for adjusting the number of intervals responsive to the filtered error signal.

8. Apparatus as defined in claim 7 wherein the circuitry for adjusting the number of intervals responsive to the filtered error signal further comprises circuitry for ensuring a correct correspondence between cycles of the reference clock and pulses of the track data clock.

9. Apparatus as defined in claim 1 further comprising:

processing circuitry for extracting digital

data from a digital data signal; and

multiplexer circuitry coupled to the sampling circuitry for selectively coupling the first and second digital data signals to processing circuitry.

10. Apparatus as defined in claim 9 further comprising:

memory circuitry for buffering the first and second digital data signals when it is not coupled to the processing circuitry by the multiplexer circuitry.

11. Apparatus of claim 10 wherein the memory circuit is a first-in, first-out memory device.

12. A method of simultaneously reading first and second data tracks of an optical disk, the method comprising a series of steps of:

providing first and second data signals corresponding to data stored in the first and second data tracks;

sampling the first and second data signals to generate first ans second digital data signals; and

synchronizing the sampling of the first and second data signals to account for variations in the linear velocities of the first and second data tracks.

13. The method as defined in claim 12 wherein the step of synchronizing sampling of the first and second data signals comprises:

providing a reference clock signal based on the first data signal; and

deriving a track data clock signal from the

reference clock signal, wherein the track data clock signal has a phase and frequency appropriate for the second data signal.

14. The method as defined in claim 13 wherein the step of generating the track data clock signal comprises:

generating track data clock pulses, wherein successive track data clock pulses are spaced apart by a number of time intervals each having a duration related to a period of the reference clock;

measuring a timing relationship between a transition of the second data signal and a preceding and a succeeding pulse in the corresponding track data clock signal; and

adjusting the number of time intervals responsive to the measured timing relationship so that subsequent transitions in the second data signal occur substantially midway between the preceding and succeeding pulses of the corresponding track data clock signal.

15. The method of claim 14 wherein the step of adjusting comprises the steps of:

generating an error signal indicative of the measured timing relationship;

filtering the error signal with a low pass filter;

adjusting the number of time intervals responsive to the filtered error signal.

16. The method of claim 15 wherein the step

of adjusting the number of time intervals responsive to the filtered error signal further comprises ensuring that there is a correct correspondence between cycles of the data clock and pulses of the track data clock.

17. The method as defined in claim 12 further comprising:

selectively processing the first and second digital data signals to extract digital data therefrom.

18. The method as defined in claim 17 further comprising:

buffering each of the first and second digital data signals when they are not being processed to extract the digital data.

19. The method of claim 18 wherein the step of buffering comprises:

converting each of the first and second digital data signals into digital data words; and

storing the digital data words in a memory device.

20. The method of claim 19 wherein the step of storing the digital data words in a memory device comprises storing the digital data words in a first-in, first-out memory device.

21. Apparatus for simultaneously reading multiple data tracks of an optical disk, the apparatus comprising:

a pickup assembly for generating plural data

signals corresponding to data stored in the multiple data tracks;

circuitry for processing the plural data signals to recover information stored on the optical disk and for storing the information to a buffer; and

circuitry operating asynchronously of the circuitry for processing for retrieving the information from the buffer and providing the information to a host processor.

22. The apparatus as defined in claim 21 further comprising:

circuitry for determining an address for a starting block of the information;

circuitry for translating the address into a predetermined one of the multiple data tracks on the optical disk; and

means for moving the pickup assembly to a location relative to the optical disk wherein the plural data signals include signals corresponding to the multiple data tracks.

23. The apparatus as defined in claim 21 wherein the circuitry for asynchronously retrieving comprises:

circuitry for determining an address for a desired block of the information;

circuitry for determining whether the desired block of information is stored in the buffer or whether the desired block of the information must be read from the optical disk.

24. Apparatus as defined in claim 21 wherein the circuitry for processing further comprises:

circuitry for multiplexing the plural data signals into a multiplexed data signal; and

circuitry for processing the multiplexed data signal to recover information stored on the optical disk.

25. Apparatus as defined in claim 21 wherein the circuitry for processing further comprises: circuitry for generating demodulated signals by performing demodulation of the plurality of data signals; and

circuitry for generating decoded signals by performing a form of Cross-Interleaved Reed Solomon code decoding of the demodulated signals.

26. Apparatus as defined in claim 22 wherein the circuitry for processing further comprises circuitry for performing error correction of decoded signals.

27. A method of simultaneously reading multiple data tracks of an optical disk, the method comprising a series of steps of:

illuminating multiple data tracks of the optical disk with plural illumination beams to create reflected illumination beams;

receiving the reflected illumination beams with a plurality of detectors to generate a plurality of data signals, each one of the plurality of detectors generating a data signal corresponding to data stored

in a corresponding data track;

processing the plurality of data signals in parallel to recover information stored on the optical disk and storing the information in a buffer; and

asynchronously retrieving the information from the buffer.

28. The method as defined in claim 27 further comprising steps of:

determining an address for a starting block of the information;

translating the address into a predetermined one of the multiple data tracks on the optical disk; and

moving the plurality of detectors to a location relative to the optical disk wherein the reflected illumination beams include the predetermined one of the multiple data tracks.

29. The method as defined in claim 27 wherein the step of asynchronously retrieving the information comprises:

determining an address for a desired block of the information;

determining whether the desired block of information is stored in the buffer or whether the desired block of the information must be read from the optical disk.

30. The method of claim 29 wherein the method further comprises a step of:

after reading the desired block of

information from the buffer, freeing up a portion of the buffer from which the desired block of information was read.

31. The method as defined in claim 30 wherein the step of processing further comprises a step of generating demodulated signals by performing demodulation of the plurality of data signals and a step of generating decoded signals by performing a form of Cross-Interleaved Reed Solomon code decoding of the demodulated signals.

32. The method as defined in claim 31 wherein the step of processing further comprises a step of performing error correction of decoded signals.

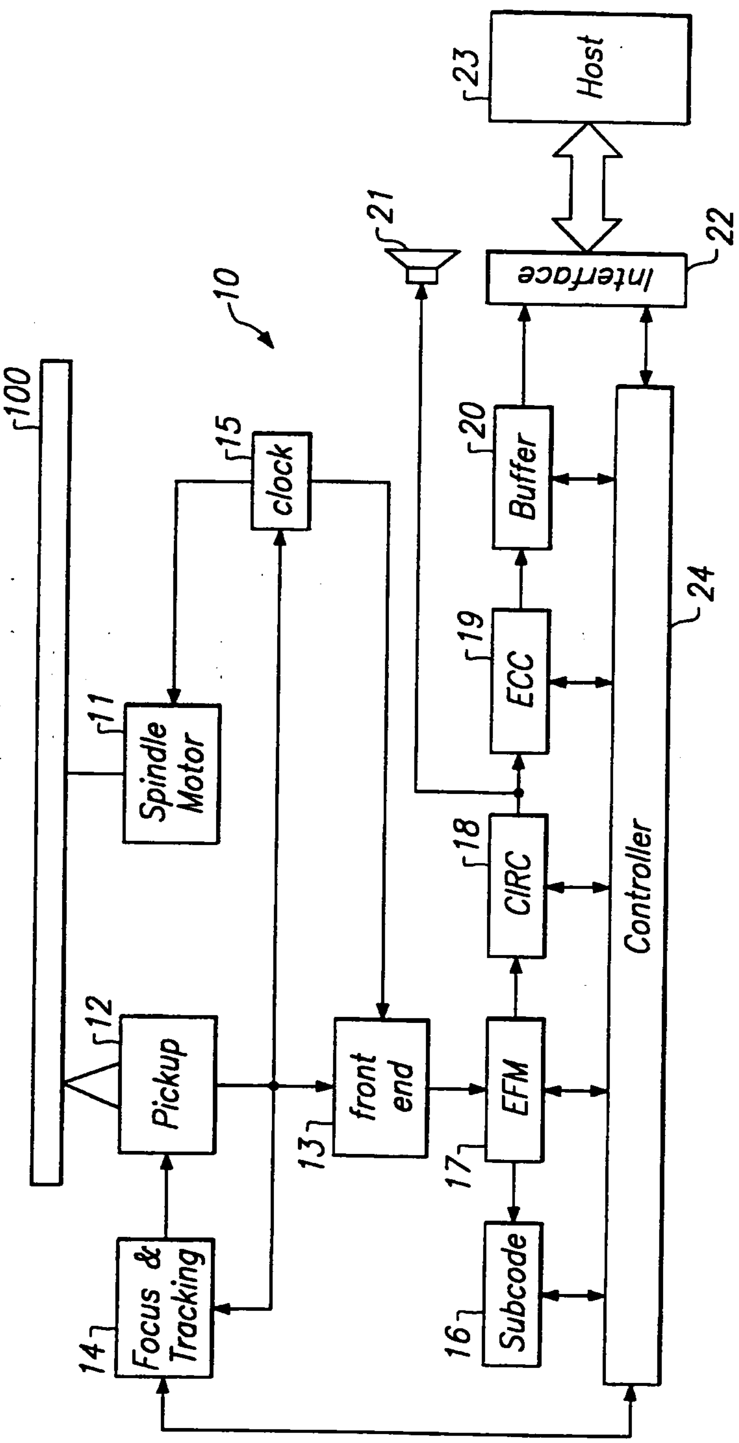


FIG. 1 (Prior Art)

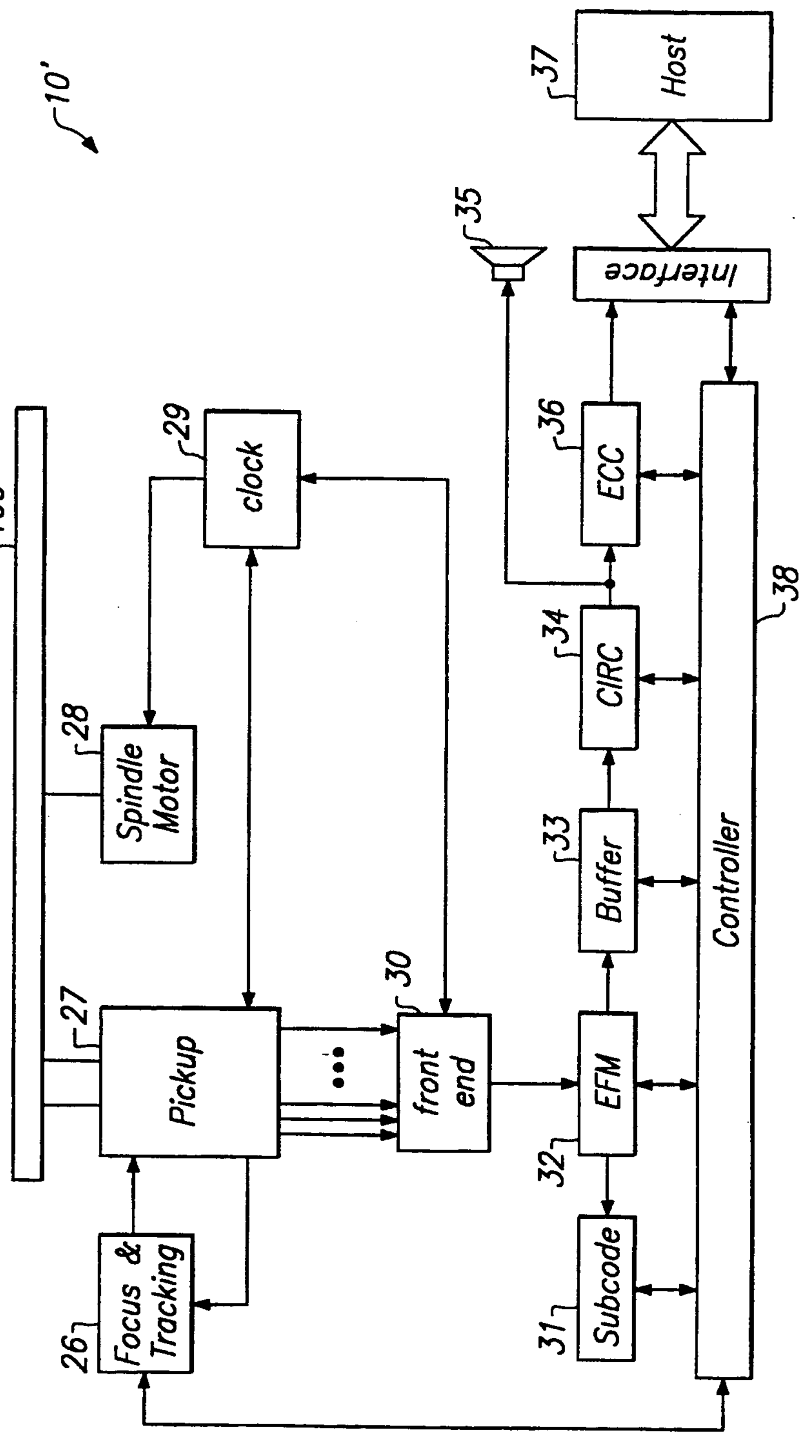

10'
100
Spindle Motor
28
clock
29
Pickup
27
front end
30
Focus & Tracking
26
Subcode
31
EFM
32
Buffer
33
CIRC
34
ECC
36
35
Interface
Host
37
Controller
38

FIG. 2

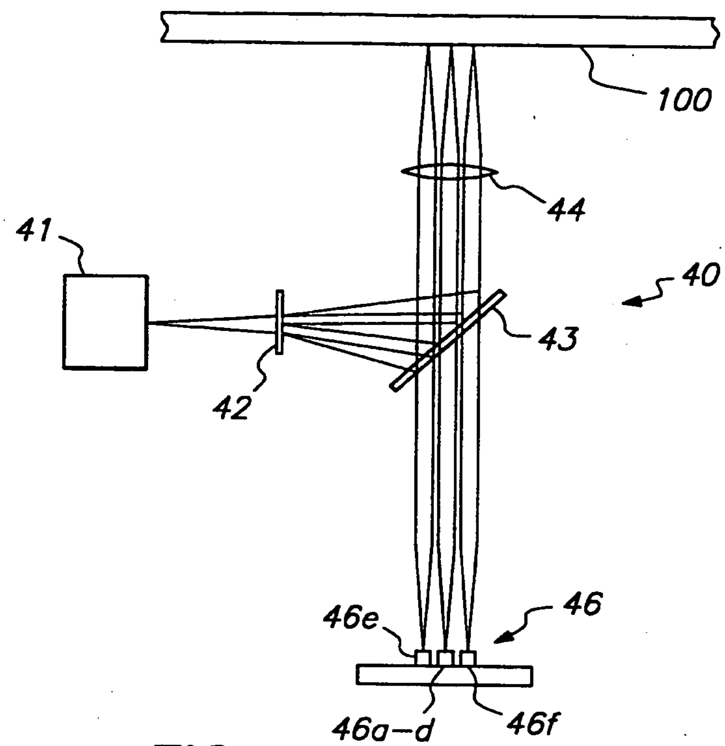


FIG. 3

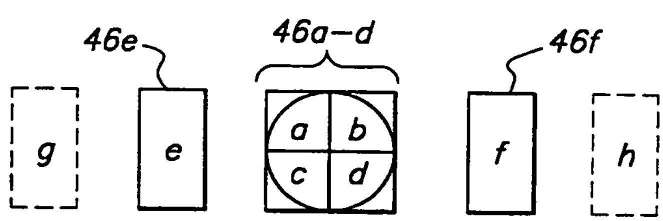


FIG. 4

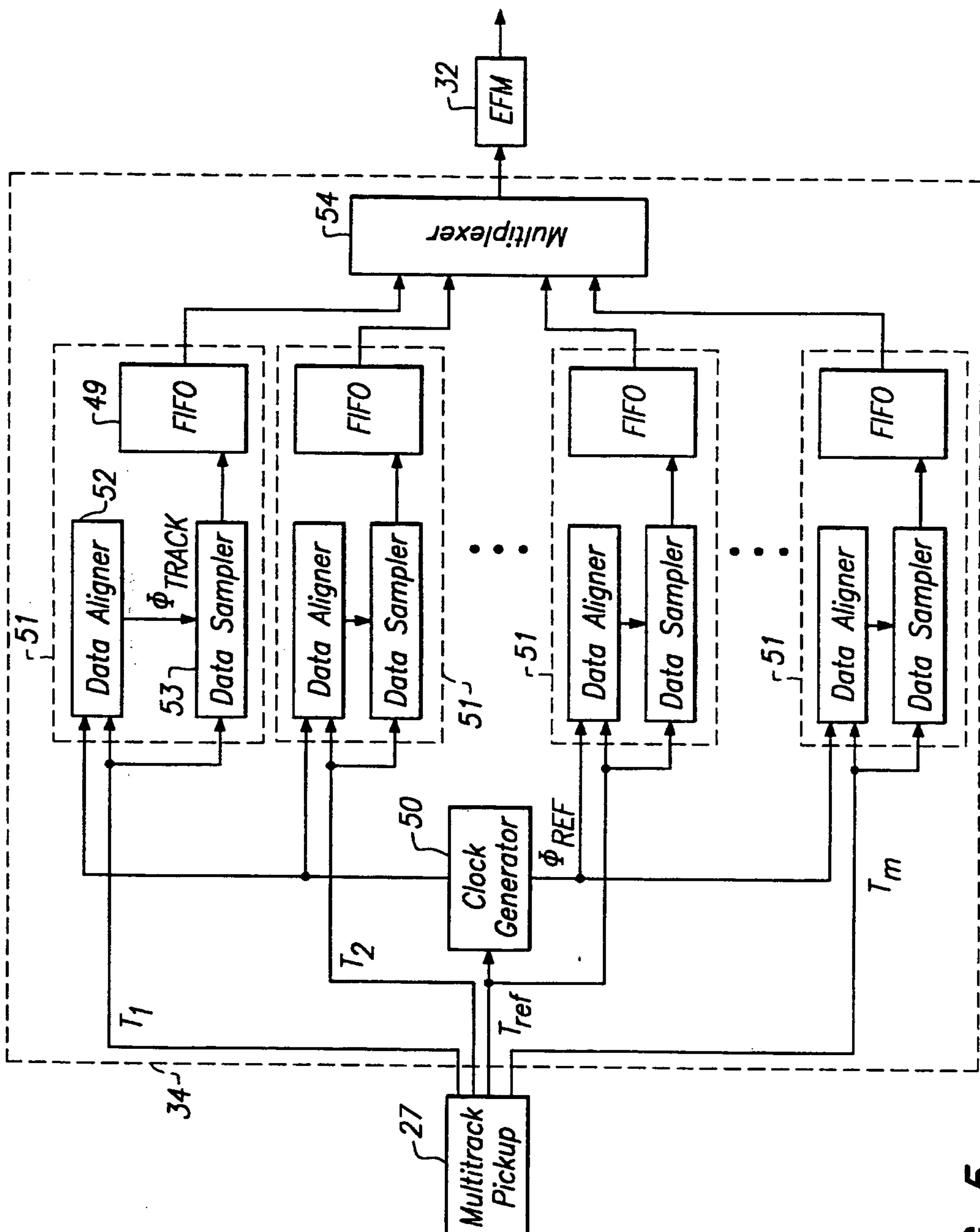
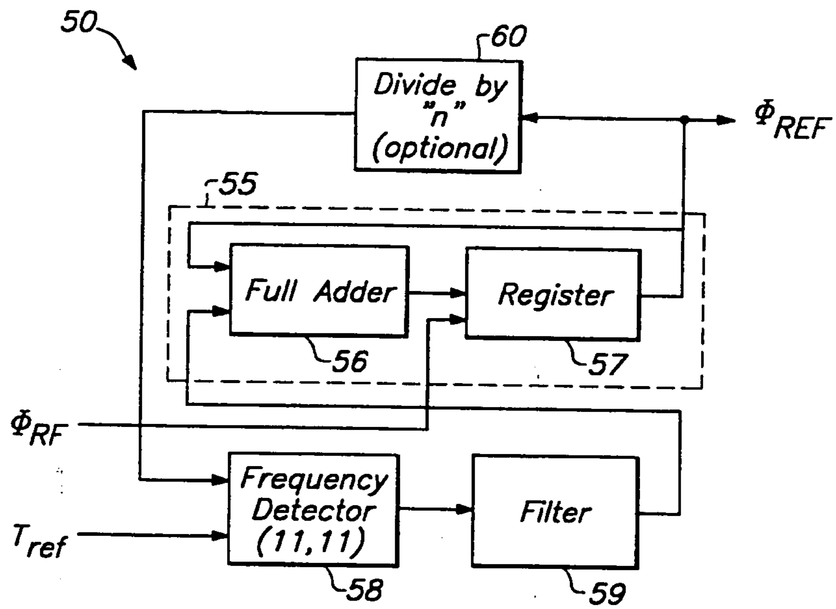
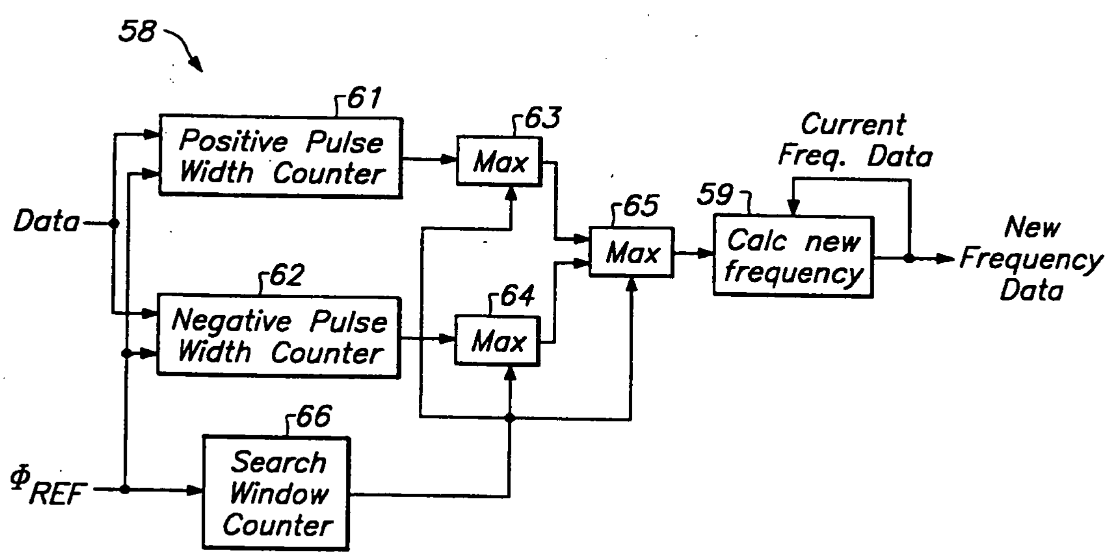

EFM
32
Multiplexer
54
FIFO
49
Data Aligner
52
Φ_{TRACK}
Data Sampler
53
51
Clock Generator
50
Φ_{REF}
T_1
T_2
T_{ref}
T_m
34
Multitrack Pickup
27

FIG. 5



50
60
Divide by "n" (optional)
Φ_{REF}
55
Full Adder
Register
56
57
Φ_{RF}
Frequency Detector (11,11)
Filter
T_{ref}
58
59

FIG. 6A



58
61
Positive Pulse Width Counter
63
Max
Current Freq. Data
65
59
Data
Max
Calc new frequency
New Frequency Data
62
Negative Pulse Width Counter
64
Max
66
Φ_{REF}
Search Window Counter

FIG. 6B

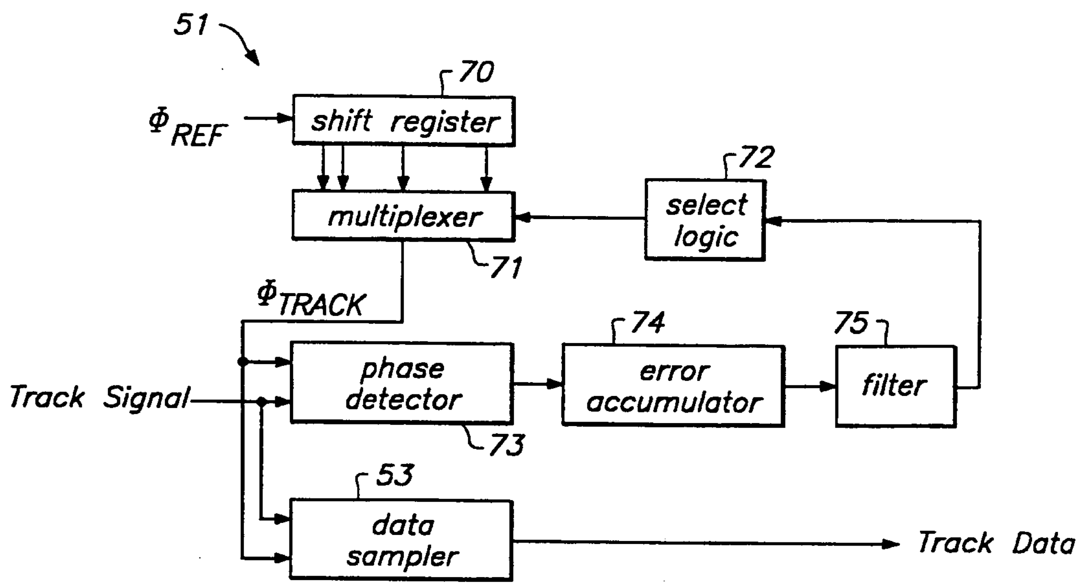

51
Φ_{REF}
shift register
70
multiplexer
71
select logic
72
Φ_{TRACK}
Track Signal
phase detector
73
error accumulator
74
75
filter
53
data sampler
Track Data

FIG. 7

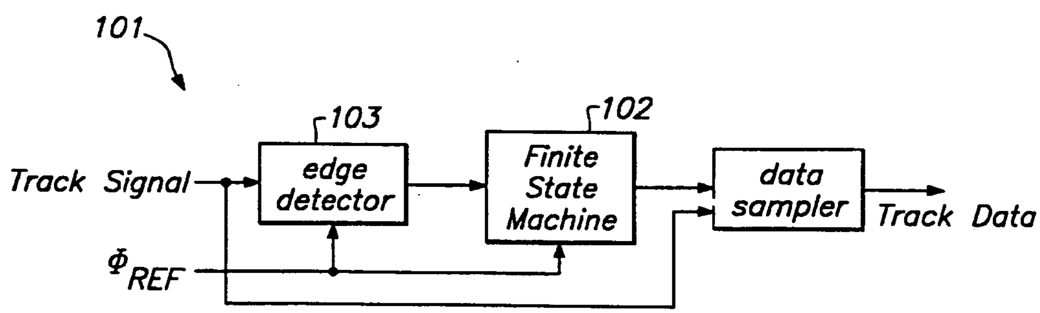

101
103
102
Track Signal
edge detector
Finite State Machine
data sampler
Track Data
Φ_{REF}

FIG. 10

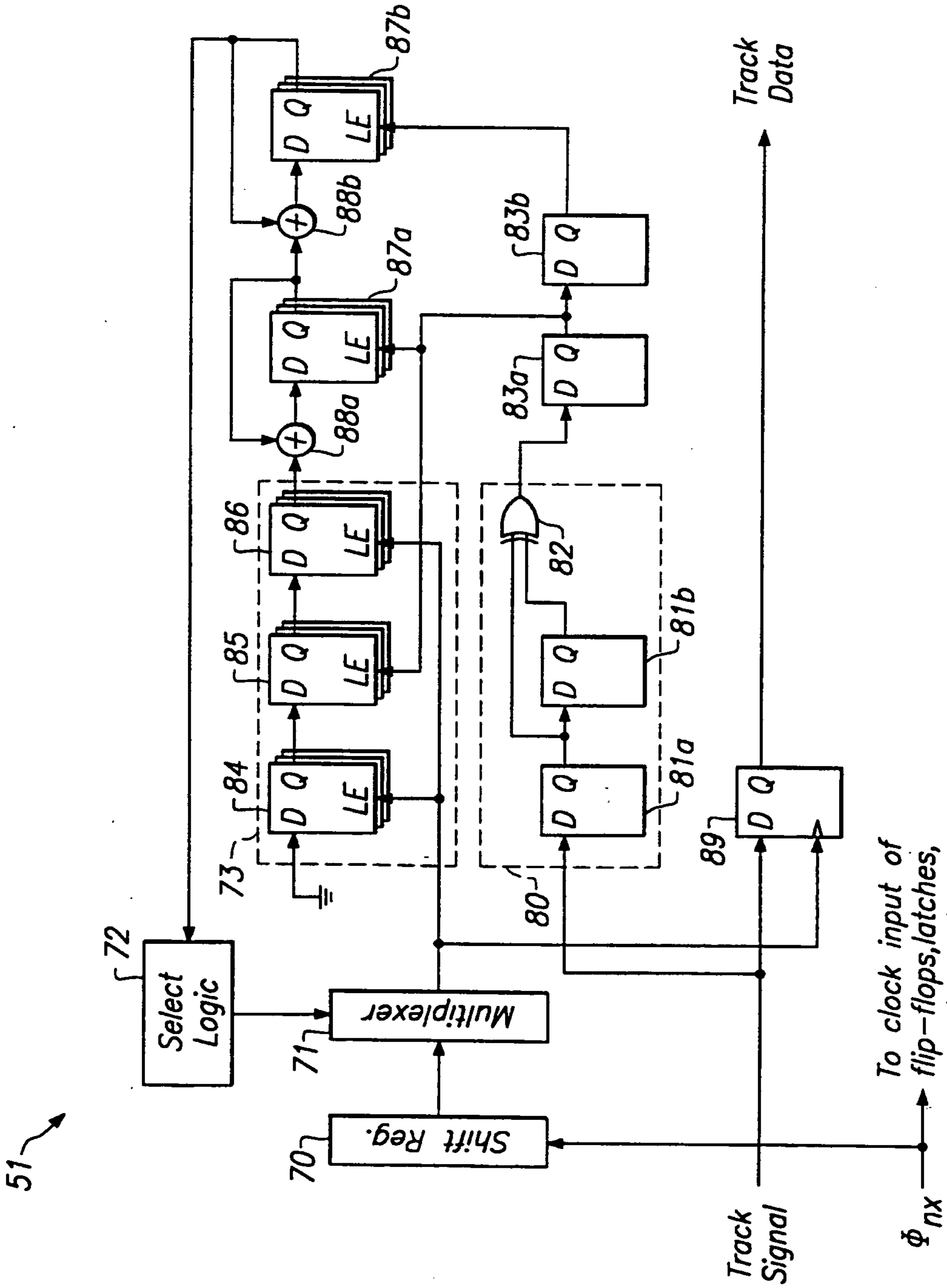

51
Select Logic
72
Multiplexer
71
Shift Reg.
70
73
84
85
86
D Q
LE
88a
87a
88b
87b
80
81a
81b
82
83a
83b
89
Track Data
Track Signal
Φ_{nx}
To clock input of flip-flops, latches, and counters

FIG. 8

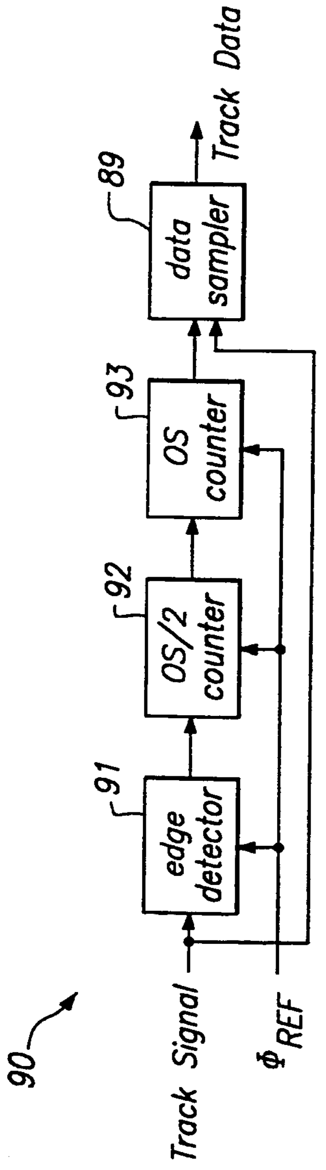

90
Track Signal
ΦREF
edge detector
91
OS/2 counter
92
OS counter
93
data sampler
89
Track Data

FIG. 9A

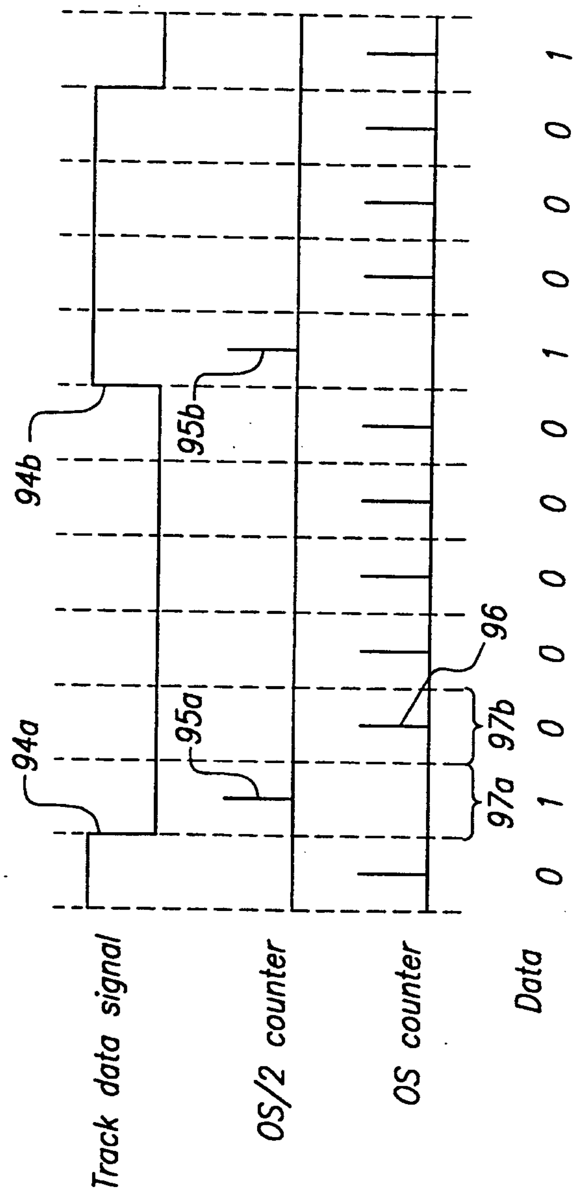

Track data signal
OS/2 counter
OS counter
Data
94a
94b
95a
95b
96
97a
97b
0 1 0 0 0 0 0 1 0 0 0 1

FIG. 9B

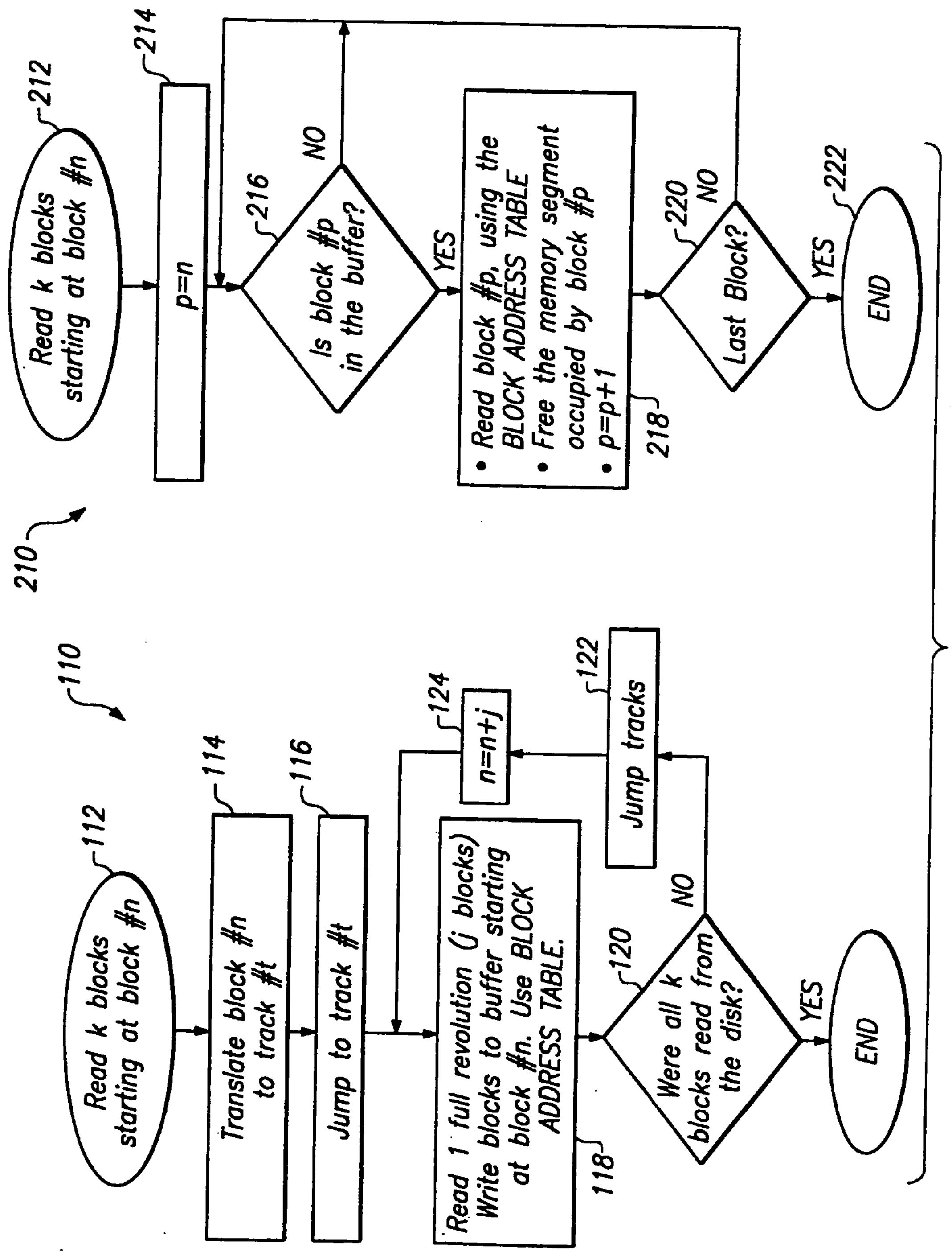

110
Read k blocks starting at block #n
112
Translate block #n to track #t
114
Jump to track #t
116
Read 1 full revolution (j blocks) Write blocks to buffer starting at block #n. Use BLOCK ADDRESS TABLE.
118
Were all k blocks read from the disk?
120
YES
NO
END
Jump tracks
122
n=n+j
124
210
Read k blocks starting at block #n
212
p=n
214
Is block #p in the buffer?
216
NO
YES
• Read block #p, using the BLOCK ADDRESS TABLE
• Free the memory segment occupied by block #p
• p=p+1
218
Last Block?
220
NO
YES
END
222

FIG. 11